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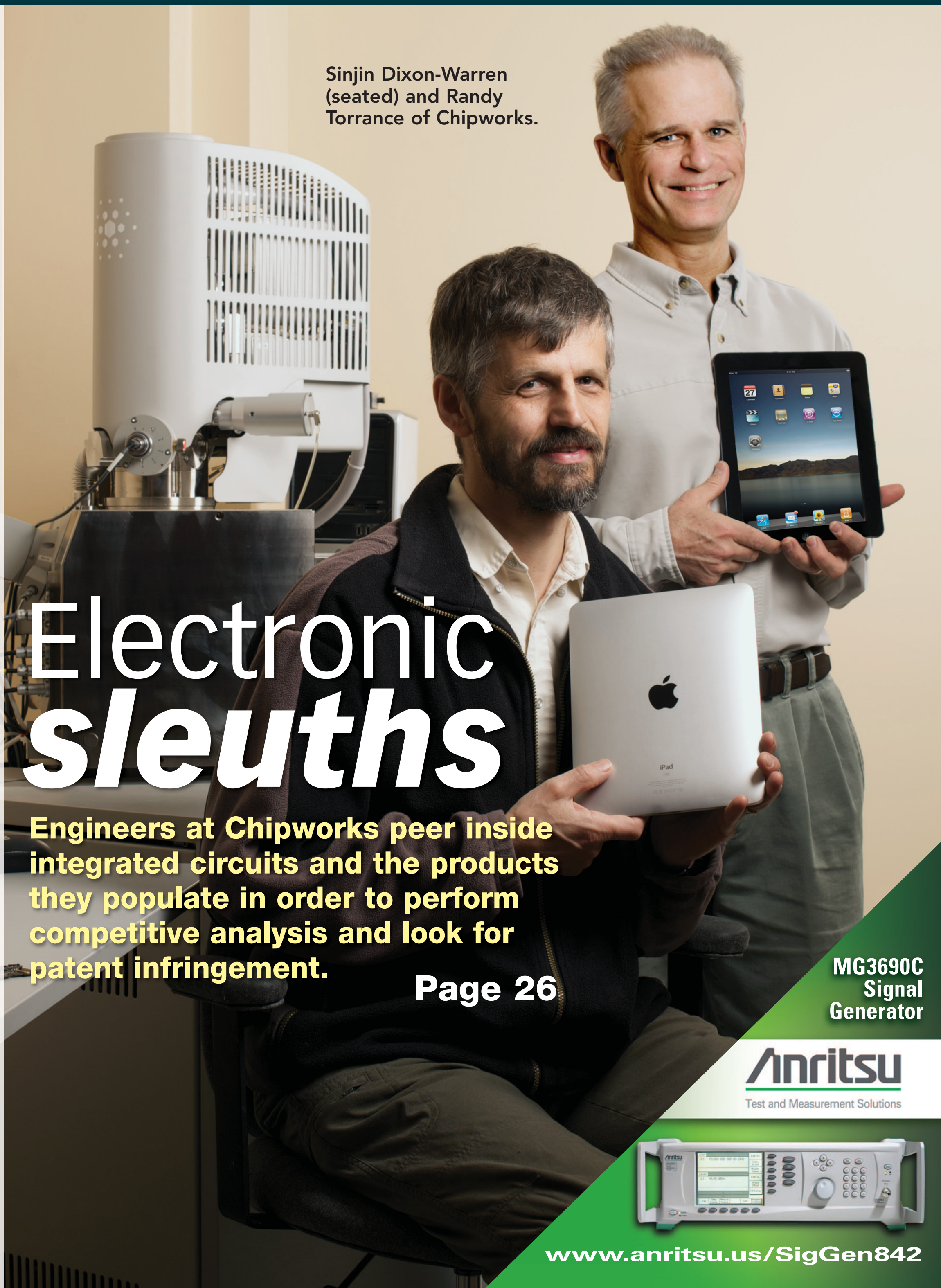
Test & Measurement World

THE MAGAZINE FOR QUALITY IN ELECTRONICS



Sinjin Dixon-Warren (seated) and Randy Torrance of Chipworks.

Electronic *sleuths*

Engineers at Chipworks peer inside integrated circuits and the products they populate in order to perform competitive analysis and look for patent infringement.

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"I need the fastest DMM they make."

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34420A	7 ½	0.0030%	250 / sec	.02 sec	GPIB, RS-232
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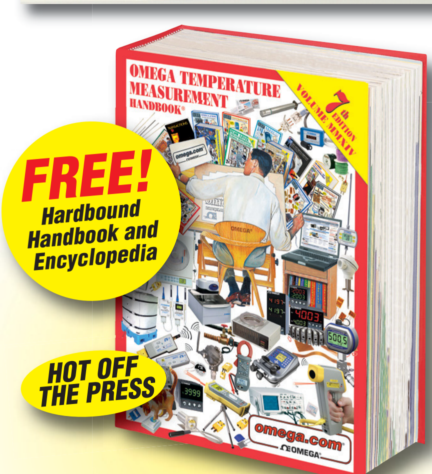

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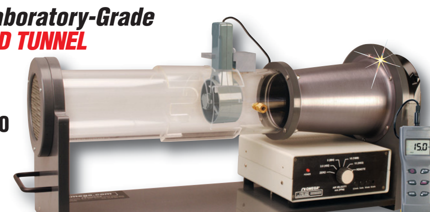

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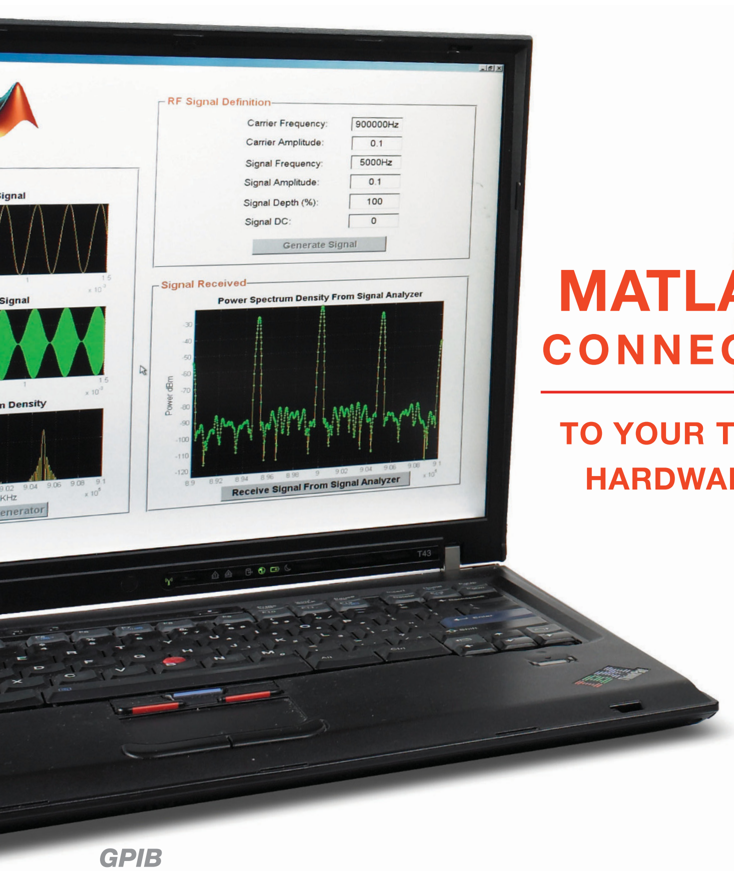

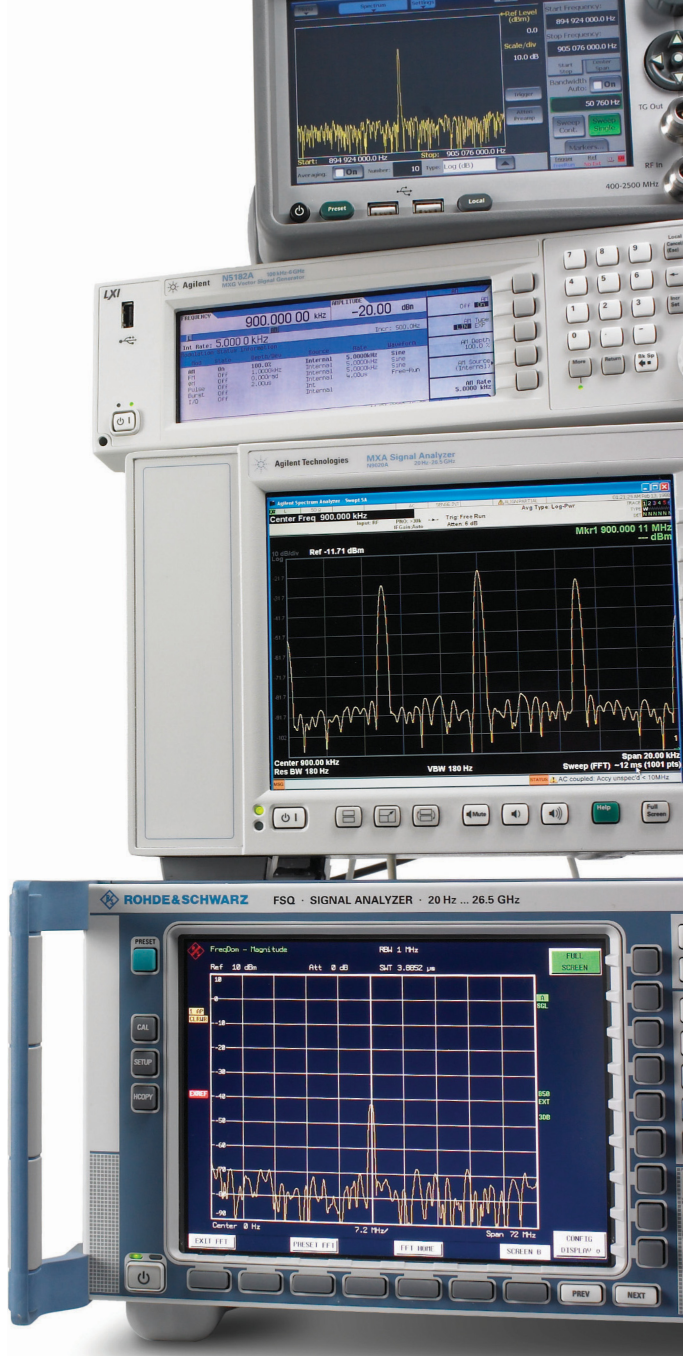

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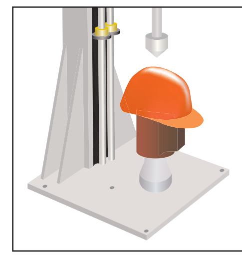

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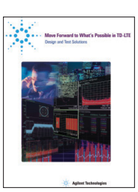

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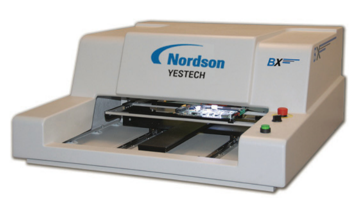

ONLINE

www.tmworld.com

Check out these exclusive features on the *Test & Measurement World* Web site:

Villanova and The MathWorks team up on mechatronics

Professor James Peyton-Jones, director of the Center for Nonlinear Dynamics & Control at Villanova University, has been working with The MathWorks on classes in mechatronics. In this interview, Peyton-Jones describes his work at the center and discusses the role The MathWorks has played in the center's efforts.

www.tmworld.com/nova_mathworks

Blog commentaries and links

Taking the Measure

Rick Nelson, Editor in Chief

- Gödel's Theorem of test
- A computer company by any other name…
- Don Quixote 2.0 is ready to install

Rowe's and Columns

Martin Rowe, Senior Technical Editor

- FCC releases RF spectrum online tool
- Should equipment companies provide repair info?
- A Carton of advice, part 5

www.tmworld.com/blogs

EDN names winners of 20th annual Innovation Awards

EDN's 2010 Innovation Awards honored a diverse group of electronics engineers and the groundbreaking products they have produced. Product awards were presented in 30 categories, including DC and low-frequency test (Agilent Technologies for the U2723A USB source-measure unit); design debug and production test (Mentor Graphics for its Tessent YieldInsight yield-analysis tool); oscilloscopes, digitizers, and data acquisition (Tektronix for the MSO70000 Series mixed-signal oscilloscopes); and RF/microwave test (Anritsu for the VectorStar microwave vector network analyzer).

www.edn.com/innovation

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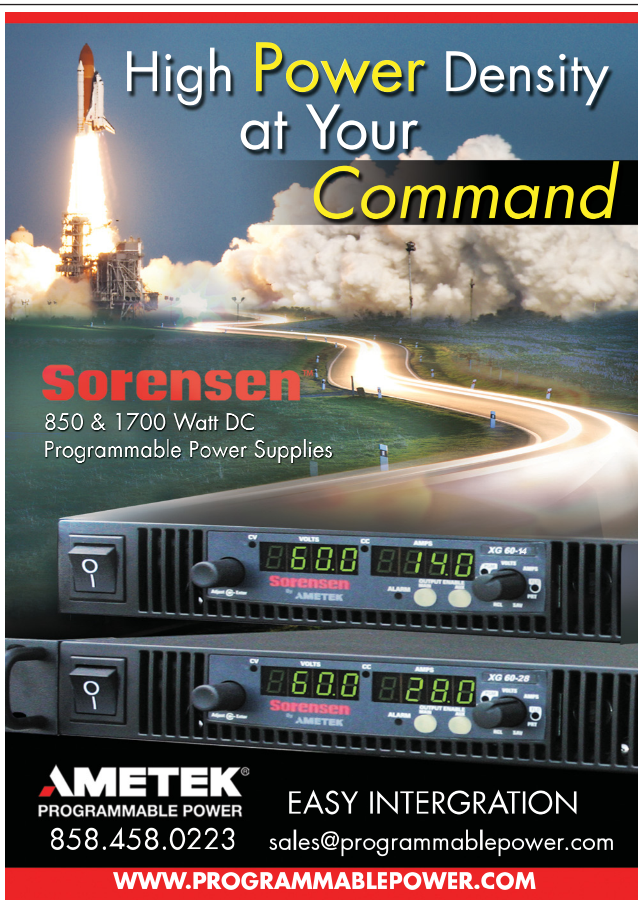

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RICK NELSON
EDITOR IN CHIEF

Recovery and jobs

The electronics industry seems poised for a strong comeback. In Q1 2010, the semiconductor industry posted a record for IC shipments in a quarter, delivering 44.5 billion units, according to IC Insights' *2010 McClean Report*. That number contrasts with the previous high of 44.1 billion units in Q3 2008 and was 59% higher than the 28 billion units shipped in Q1 2009.

It would seem that the news must be equally good for the OEMs buying those chips and the test and measurement companies that ensure the quality of the chips and end products they populate. Similarly, the picture should be good for employment.

Share your thoughts on employment at a DAC panel discussion on June 14.

That's not necessarily the case, however. On May 11, Carey Gillam of Reuters reported from the Manufacturing and Transportation Summit in Chicago that "U.S. payroll numbers may be starting to improve, but leaders from a cross-section of manufacturing and transportation companies...remain reluctant to hire too many workers too soon."

It's not just manufacturing jobs that will see sluggish growth. Barriers remain to engineering job growth, at least in the US. In a recent interview, Silvina Grad-Freilich, parallel-computing marketing manager at The MathWorks, suggested that parallel computing promises to make engineers more productive. Unfortunately, that can lead employers to conclude that it's cheaper to add processor cores or augment computer clusters than it is to hire engineers.

Another problem is that the US may be losing its competitive edge—an issue I addressed in my editorial in the May 13 issue of sibling publication *EDN*. As evidence, many of the companies winning *EDN* Innovation Awards in April had deployed multinational engineering teams to earn their awards.

Further evidence that US engineers don't have a monopoly on innovation was Intel's announcement in April that it plans to invest $177 million over the next three years to expand its Guadalajara, Mexico, design center. Intel CEO Paul Otellini made the announcement during a press conference with Mexico President Felipe Calderon. The investment will focus on technology development activities and education initiatives that support Calderon's National Digital Plan.

The expansion at Intel GDC (Guadalajara design center) will include the construction of labs, office space, and a technology museum for children. Intel also estimated that approximately 150 technical jobs will be created over three years, bringing the total number of GDC engineers to 550.

"As a global computing leader, we believe that investing in the future of discovery is an essential business decision," Otellini said. "Our team in Mexico will continue to help us do this. This new investment today extends our long-term commitment to Mexico."

If US-based engineering employment is to grow, US engineers will have to successfully compete with their counterparts, such as the designers at GDC, in other countries. And US companies will need to deploy enhancements like parallel computing tools to vastly expand their innovative efforts—not simply to do a little more with the same number of engineers.

I'll be moderating a panel titled "Career Outlook: Job Market 2010" June 14 at the Design Automation Conference. Come and share your thoughts on employment and innovation. T&MW

> > > POST YOUR COMMENTS AT WWW.TMWORLD.COM/BLOG.

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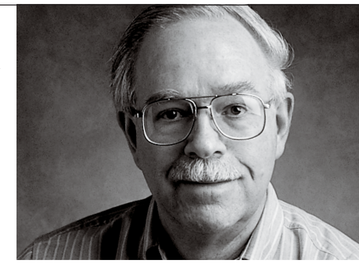

A few pounds of parts

Frequent readers of this column may recall that I volunteer at WinCycle, a nonprofit electronics-recycling facility located in Windsor, VT. When a local firm went out of business and abandoned several hundred pounds of mixed electronic components, the property's new owner delivered them to WinCycle after attempting and failing to find a buyer for the lot.

The mélange comprised mostly leaded resistors, capacitors, and semiconductors, all of pre-RoHS origin and either loose or falling out of crumbling plastic bags. A smattering of dried insects and Vermont warehouse dust topped off the batch. Sorting and repackaging the lot would have taken months, but these obsolescent components were still usable and too good to recycle as scrap metal.

Lyle Patterson, WinCycle's facilities manager, suggested that we find someone to whom we could donate the components. I contacted local amateur-radio clubs and publicized a series of open-house events in which radio amateurs were invited to visit and take home whatever they could use. Over several weeks, only a dozen or so showed up.

To reach a wider audience, I offered the parts to a couple of amateur-radio newsgroups that emphasized radio-equipment construction. Requestors would pay for a flat-rate US Postal Service Priority Mail package and receive approximately 10 lb of randomly mixed parts.

We encouraged radio amateurs who were unemployed, disabled, living on fixed incomes, or located far away from hamfests and other sources of parts to request packages. By the time we ran out of components, we had shipped 112 packages to most of the US, including Hawaii and Alaska—that's more than 1000 lb of usable parts delivered into the hands of radio amateurs of all ages and skills who build their own equipment and thus learn about electronics. Sorting and identifying components just might inspire future test and reliability engineers, too.

Before your company trashes a stockroom full of obsolete components, why not give them away instead? They're worth more in the hands of hobbyists than as smelter feedstock. In addition to amateur-radio enthusiasts, those robot builders, electronic-music constructors, and budding microprocessor hackers might be your future employees—and customers! T&MW

To read past "Test Voices" columns, go to www.tmworld.com/testvoices.

HOBBYISTS AND COMPONENTS

Where can you find hobbyists? Begin by asking at your workplace—odds are, any collection of electronics workers worth its salt includes at least one radio amateur who attends radio club meetings or communicates with other hams on the air or via the Internet. Ask teachers and youth group leaders whether they know of likely recipients, or sponsor your own robotics or radio club. The American Radio Relay League has a list of amateur clubs:
www.arrl.org/clubs

To review the details of WinCycle's component giveaway, go here:
mail.qrp-l.org/pipermail/qrp-l_qrp-l.org/2010-January/017259.html

Traveling pants? No. Traveling junkbox? Yes. For years, electronics experimenters have been shipping cartons of surplus parts from place to place. An originator fills a package with excess parts and mails it to a recipient who removes needed parts, replaces them with surplus parts, and sends the package to the next recipient. For details, go to these two sites:
4hv.org/e107_plugins/forum/forum_viewtopic.php?48923
www.savagecircuits.com/forums/showthread.php?108-Fellowship-of-the-Traveling-Junkbox

To banish any doubt that electronics experimentation is alive and well, visit:
www.electronics-lab.com

If you maintain Heath test equipment, this site cross-references Heath part numbers and functions to standard designations. Also available are schematics and manuals for non-Heath equipment:
www.tech-systems-labs.com/heathkitparts.htm

If you must repair a Hewlett-Packard laser printer instead of salvaging it, this site offers diagnostics and repair tips:
www.mj-printers.com/repair/techsupport.html

LeCroy debuts embedded-test tools

LeCroy took aim at the test of embedded systems with its introduction of its ArbStudio AWG (arbitrary waveform generator) series and LogicStudio 16 logic analyzer at the Embedded Systems Conference, April 26–29 in San Jose.

The ArbStudio AWG (pictured) generates signals up to 125 MHz and includes pulse-width-modulation capabilities. The software interface that controls the hardware simplifies waveform creation with a navigation tree that allows easy access to all channels.

The ArbStudio series includes four models: two- and four-channel versions with analog waveform capabilities plus two- and four-channel versions offering a combination of analog waveform and digital pattern-generation capabilities. The four-channel models have an expansion port that allows up to eight units to be connected. All models have a 125-MHz bandwidth, 1-Gsample/s maximum sample rate, 2 Mpoints/channel memory, and 16-bit resolution. The instruments support both true arbitrary and DDS (direct digital synthesis) technologies. ArbStudio software runs on an external PC. Base price is $2490 to $4990.

The LogicStudio 16 brings logic-analyzer functionality to a PC, providing 16 channels with a sample rate of 1 Gsample/s and a maximum input frequency of up to 100 MHz. LogicStudio 16 software provides a dynamic waveform display with an intuitive user interface. Tools for digital debug include timing cursors, zooming and panning functions, a persistence display, and a history mode that can replay old data captures. LogicStudio supports protocol analysis for I2C, SPI, and UART interfaces. It can trigger on specific bus addresses or data packets. LogicStudio provides a communication link to LeCroy's WaveJet oscilloscope, thereby turning a PC in to a mixed-signal debug environment. Base price is $990. www.lecroy.com.

Tektronix acquires SyntheSys Research

Tektronix (a division of Danaher) has acquired SyntheSys Research, a manufacturer of high-speed signal-integrity test instruments. SyntheSys Research is probably best known for its BERTScope signal-integrity analyzer. "The combination of SyntheSys and Tektronix accelerates our ability to provide leading full product solutions for both transmitter and receiver high-speed serial test," said Brian Reich, GM of performance oscilloscopes for Tektronix, in a prepared statement. www.tektronix.com.

Agilent and UCSD collaborate on chip-scale photonic test facility

Agilent Technologies has partnered with the UCSD (University of California, San Diego) to establish a test facility for chip-scale micro and nanophotonic devices. The facility is part of the NSF MRI (National Science Foundation Major Research Instrumentation) project and is being set up in conjunction with the multi-university CIAN (Center for Integrated Access Networks).

The facility, which is housed on the UCSD campus, will support testing of micro- and nanoscale ultra-high-speed optical components and subsystems. A suite of 40-Gbps test equipment will permit component-level compliance testing and troubleshooting of devices intended for NSF's MRI Data Center Testbed. In the next few years, CIAN participants expect to upgrade the basic data rates of the chip-scale photonic testing facility to 100 Gbps. The facility also will add system-level and network-level analysis capabilities. www.agilent.com.

Editors' CHOICE

PoE compact vision system

ADlink Technology had announced the release of the EOS-1000 compact vision system, based on the Intel Core2 Duo P8400 processor. The EOS-1000 provides four independent PoE (Power over Ethernet) ports with data-transfer rates up to 4.0 Gbps and combines high computing power with multi-camera imaging.

The EOS-1000 measures 7.8x6.5x3.3 in. and can tolerate vibrations of up to 5 g. It incorporates circuitry to monitor CPU temperature, fan speed, and system responsiveness to enhance reliability. The PoE technology featured on the EOS-1000 allows power to be supplied through the Ethernet cables spanning distances up to 100 m. The EOS-1000 also provides an auto-detection function to ensure compatibility with both PoE and conventional non-PoE devices.

The EOS-1000 also features multiple I/O options, including two RS-232/485 ports, four USB ports, 32 isolated digital lines, and dual storage options (HDD and CompactFlash).

Price: $1635. *ADlink Technology, www.adlinktech.com.*

CALENDAR

Semicon West, July 13–15, San Francisco. *SEMI, www.semi.org.*

EMC Symposium, July 25–30, Ft. Lauderdale. *IEEE, www.emc2010.org.*

NIWeek, August 3–5, Austin. *National Instruments, www.niweek.com.*

Autotestcon, September 13–16, Orlando. *IEEE, www.autotestcon.com.*

International Test Conference, November 2–4, Austin. *IEEE, www.itctestweek.org.*

To learn about other conferences, courses, and calls for papers, visit www.tmworld.com/events.

Editors' CHOICE

Data-acquisition logger stands alone

Multifunction data-acquisition systems, with analog and digital inputs and counters, often require a PC. The LGR-5320 series from Measurement Computing doesn't. You can program it from your PC, then download the configuration data into the module for stand-alone operation.

The three models in the LGR-5320 series have eight differential/16 single-ended 16-bit analog inputs, 16 digital inputs, four counter inputs, and a relay output. For analog inputs, the two higher-end models sample at 200 ksamples/s; the third module samples at 100 ksamples/s. All models come with a 4-Gbyte SD memory card, but you can use SD cards that hold up to 32 Gbytes.

You can instruct the modules to log data either by using a push-button or by using triggers. The LGR-5329 and LGR-5327 can trigger an acquisition based on analog levels across multiple channels, or you can trigger on a combination of digital inputs, but not both. The LGR-5325 can trigger on a single analog or digital channel. You can program a trigger length based on number of samples or time duration, then re-arm the trigger.

Prices: LGR-5325—$1499; LGR-5327—$1799; and LGR-5329—$2199. *Measurement Computing, www.mccdaq.com.*

APEX helps engineers contend with ever-denser PCBs

> > > IPC APEX Expo, April 6–9, 2010, Las Vegas, NV, www.ipcapexexpo.org.

Design and test hardware and software combined with optical and x-ray inspection equipment at IPC APEX Expo. Offering the gamut of test inspection was **TRI** (Test Research Inc.), which displayed its end-to-end test systems for SMT manufacturing, including systems for each phase of the manufacturing process from SPI (solder paste inspection), to AOI (automated optical inspection), AXI (automated x-ray inspection), and ICT (in-circuit test).

Agilent Technologies showcased its Medalist i3070 Series 5 in-circuit tester, which boosts throughput and includes a power-monitoring circuit to protect ICs. Agilent also highlighted its i1000D low-cost digital in-circuit tester, and it exhibited the heretofore not highly publicized TS-5040 functional tester, which works with Agilent's TestExec SL 6.1 software.

In conjunction with Agilent, **Aster Technologies** introduced what it calls the first design-for-test software tool to combine electrical and mechanical analysis. The new tool consists of a "probe analyzer" enhancement to Aster's TestWay coverage-analysis tool. The probe analyzer is an interactive, rules-based routine designed to assist the layout engineer or test developer in identifying usable PCB (printed-circuit board) locations for physical access.

Texmac, the exclusive authorized distributor of **Takaya** flying probers in North America, demonstrated the Takaya APT-9411SL, which the company said is designed to test the large, technically advanced PCBs employed in US telecommunications, high-end-computing, and defense-electronics industries. **Everett Charles Technologies** debuted its ZOOM fixture, which is designed for ultra-fine-pitch probing of loaded PCBs and can test down to 24-mil (0.6-mm) centers and 15-mil diameter targets. Everett Charles also highlighted its MetriX probes for close-center probing of loaded PCBs.

Acculogic featured its FLS 980Dxi Flying Scorpion, a double-sided, 16-probe flying-probe system with 3-D probing, analog, digital, and boundary-scan test capability on all probes (top and bottom side). **Goepel Electronic** introduced new features designed for parallel execution of its VarioTAP processor emulation with its System Cascon boundary-scan software platform. Goepel also announced the development of VarioTAP model libraries for Xilinx FPGAs with integrated PowerPC cores.

Koh Young Technology highlighted its new Zenith 3-D AOI system, which offers true 3-D AOI through its ability to measure the z-axis profilometry of assembled PCB surfaces based on patented multi-frequency moiré technology. **Nordson DAGE** presented its XD7600NT100HP x-ray inspection system, which offers 100-nm feature recognition.

Texmac demonstrated the Takaya APT-9411SL, which the company said is designed to test the large, technically advanced PCBs employed in US telecommunications, high-end-computing, and defense-electronics industries. Base price is less than $300,000. Courtesy of Takaya.

CyberOptics introduced the SE350 addition to its 3-D SPI system portfolio. The SE350 employs CyberOptics calibration-free sensor technology. **SiFO Technology** launched its Independence test-services program, under which the company, headquartered in Suzhou, China, targets US OEMs who employ contract manufacturers in China and other Asian countries to build their products. Also focusing on services, **NBS** showcased the portfolio of engineering and manufacturing services that it offers at its Santa Clara headquarters.

Aegis Software announced what it calls an industry-first OEM bundling agreement with **Fuji America.** Under this agreement, Fuji America will include Aegis NPI software for BOM (bill of materials), CAD, Gerber, and even scanned-board data conversion with each license of Fuji Flexa software. In addition, Aegis announced its software's selection and deployment as the global manufacturing process software for Sanmina-SCI.

Finally, **3M** highlighted initiatives related to embedded capacitance material, used in backplanes, PCBs, modules, and chip packages to provide improved electrical performance, space reduction, electromagnetic interference reduction, and reliability improvement. T&MW

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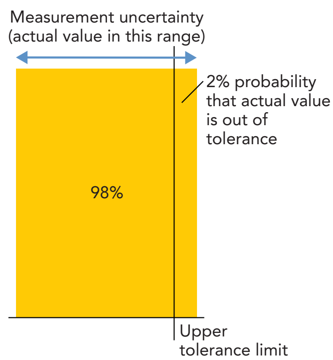
Calibration is changing

The calibration and metrology profession hardly seems to change. In this business, engineers treat the latest measuring instrument with suspicion until it has a proven, documented track record. Yet, changes do take place, although perhaps more slowly than in other fields. Two significant issues have recently emerged, one driven by a document, the other by economics.

ANSI/NCSL Z540.3 section 5.3 (Ref. 1) addresses the risk of false acceptance. The probability of accepting an out-of-tolerance part can't exceed 2% (**figure**). Arriving at that number involves knowing the uncertainty of the measurement, which is directly tied to TUR (test uncertainty ratio).

Howard Zion, director of technical operation at Transcat, advises clients on how PFA (probability of false acceptance) affects their manufacturing procedures. "The conversation takes anywhere from 30 minutes to four hours," he said. "Engineers outside of the calibration community are starting to understand the importance of measurement uncertainty."

Ultimately, it's up to you to decide how much risk is acceptable. The amount of acceptable risk depends on the consequences of passing bad parts. For example, if a measurement should fall at its tolerance limit, then the probability that the measurement is out of tolerance is 50%. Depending on the part,



Compliance to ANSI Z.540.3 requires that the probability of false passing is less than 2%.

you may need to add guardbands around your measurements to increase the probability that the actual value falls within tolerance. In some instances, a 2% PFA might be too high. (The online version of this article includes links to papers that describe PFA and how to determine risk, www.tmworld.com/2010_06.)

The second shift has occurred as companies have moved calibration of measurement equipment closer to manufacturing. Measurement consultant Charles Motzko noted that the practice started at TRW (now Northrop Grumman) before being adopted by other aerospace companies and eventually by other industries. Moving calibration closer to manufacturing may mean less downtime, because the equipment is calibrated in place rather than returning to the cal lab.

This shift has changed the way companies view metrology, which has traditionally been treated as a separate technical function. "Moving calibration to the manufacturing floor means you must teach engineers and technicians how to measure," said Motzko. "Measurements can no longer be a specialty."

In addition, the use of automated calibration tools means that calibration may be performed by less skilled people than in the past. Even so, there's a concern that industry won't have enough people trained in calibration and metrology. "The skill set is down," said Steve Griffin, president of Workload Tools and director of the 2010 NCSLI Workshop and Symposium. The problem will likely increase as engineers with measurement expertise retire—they'll take their knowledge with them.

To address the problem, NCSL International has a program to pique interest in calibration and metrology. The NCSLI Committee on Education Liaison and Outreach works with colleges that offer programs in measurement. NCSLI has also distributed a DVD called "Find a Cool Career in Metrology" to its members. You can learn more about the program at www.ncsli.org. Click on "Learning and development." T&MW

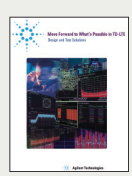
REFERENCE

1. ANSI/NCSL Z540.3-2006, "Requirements for the Calibration of Measuring and Test Equipment," NCSL International. www.ncsli.org.

Learn phase noise and harmonics

"Comparing Spectral Purity in Microwave Signal Generators" from Gigatronics give you an overview of how phase noise and harmonics add distortion to all microwave signals. The paper explains how to interpret these specifications. www.gigatronics.com.

LTE test resources available online



The Agilent Technologies Website offers a series of app notes, posters, Webcast CDs, and brochures on LTE testing. Topics include design and test fundamentals, stimulus response testing, and MIMO test. www.agilent.com/find/LTE-forward.

CD explains measurements

Keithley Instruments' "A Guide to Understanding Electrical Test and Measurement" CD contains app notes, white papers, and Webcasts about instruments such as multimeters, source-measure units, and waveform generators. www.ggcomm.com/Keithley/Mar10_NewsRelease_GeneralMeasCD.html.

[EMBEDDED INSTRUMENTATION]

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Solving accessibility issues

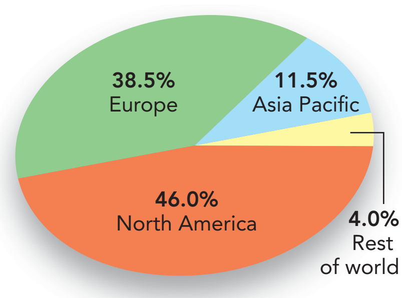
Test equipment such as in-circuit testers and manufacturing defect analyzers have successfully met end-user requirements in the past, but they are less successful at accessing the data points on today's complex smart chips. Some of the complicating factors include:

- the lack of test access for signal-integrity testing,
- the migration to chip-interconnect speeds in excess of 5 Gbps, and
- the need for protocol-aware, high-speed I/O test.

Vendors, therefore, need to develop better solutions for measuring and testing devices. Embedded instrumentation is the answer to these problems.

Embedded instrumentation is a concept of entrenching the capabilities of traditional external test equipment as a resource on a chip or circuit board. Then, through industry-standard access mechanisms, software is used to run the instrument and collect data for analysis.

Two emerging standards are expanding the possibilities of embedded instrumentation: IEEE 1149.7 and IEEE P1687. IEEE 1149.7 describes circuitry that can be added to an IC to provide access to Test Access Ports defined in IEEE 1149.1 (JTAG). IEEE P1687, or Internal JTAG, is expected to leverage the infrastructure defined in IEEE 1149.1 to access and control on-chip test circuitry. These standards are expected to enhance the use of embedded instrumentation in the near future for testing and validating 3-D multiple-die chip packages, which some predict will become a prevalent technology and allow the industry to keep up with Moore's Law in the future.



North America contributed 46.0% of the market revenues in the boundary-scan testing equipment market in 2008.

The IEEE 1149.7 standard is adaptable to TSVs (through-silicon vias), which are essential for 3-D die-stacked chips. Enhancements to IEEE 1149.7 over IEEE 1149.1 also make it effective for testing and validating 3-D chips. With access provided to embedded instrumentation by IEEE 1149.7 and IEEE 1149.1, the IEEE P1687 standard can manage and control those instruments and facilitate the correlation of the test results.

Our market research leads us to expect the boundary-scan test market to grow the fastest among all types of legacy test technologies. The in-circuit test market had revenues of $354.7 million in 2008, a growth rate of 4.7% over the previous year, with growth rates expected to decelerate as other technologies take shares from this segment. Manufacturing defect analyzers had revenues of $130.7 million in 2008, a growth rate of 5.3% from 2007; growth rates in this market are expected to remain relatively flat.

Although the boundary-scan test equipment market registered revenues of only $28.8 million in 2008, this represented an increase of 8.6% over 2007. The compound annual growth rate for this market is expected to be 8.5% from 2008 to 2013.

As manufacturers remain concerned about capital expenditures in this downturned market, one benefit of boundary scan is its fairly low entry cost—a tester costs in the $10,000 to $40,000 range. Boundary scan is also less expensive than older probe-based technologies because it is more software oriented. T&MW

To read past "Market Trends" columns, go to www.tmworld.com/markettrends.

Foundry revenue gains to outperform semiconductor industry gains in 2010

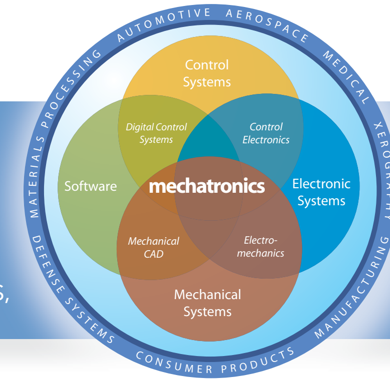
Things are looking up for foundries. With foundry revenue expected to grow by nearly 40% in 2010, revenue expansion in the foundry business is forecast to outperform that of the semiconductor industry this year, according to a recent report from iSuppli, which estimates pure-play foundry suppliers will see revenues in 2010 increase 39.5%.

The forecast expects pure-play foundry revenue to reach $24.8 billion this year, up from $17.8 billion in 2009 and up 24.6% from 2008 levels of $19.9 billion. By 2013, iSuppli said it expects foundry revenue will reach $35.9 billion with a CAGR (compound annual growth rate) of 12.5%. Earlier, iSuppli estimated semiconductor industry revenue will rise 30.6% from 2009's $229.9 billion to $300.3 billion in 2010.

"Lured by innovative new features and a renewed economy, worldwide consumers again are purchasing electronic products," said Len Jelinek, director and chief analyst for semiconductor manufacturing at iSuppli, in a statement. "Unless conditions deteriorate once more, previously pent-up need for new consumer products will fuel foundry demand, iSuppli believes."

ISuppli noted that growth won't be limited to the leading foundry vendors but will also extend to specialty foundries.

Suzanne Deffree, Managing Editor, News, EDN



Handling the wide world of webs

Before the Internet, engineers were handling webs at astonishing speeds.

Kevin C Craig, PhD
Robert C. Greenheck Chair in Engineering Design & Professor of Mechanical Engineering, College of Engineering, Marquette University.

For more mechatronic news, visit: mechatronicszone.com.

The word "web" means different things to different people. To some, it conjures up images of Spider-Man, while for others, it is the World Wide Web. For many engineers, however, the word web brings to mind the pervasive material web used in processes that make the majority of the products we all use. This material-handling application is indispensable in so many diverse industries, yet it is often overlooked. There is also often a gap and a time lag between the latest technological advances in web handling and actual industrial practices.

The economic advantage of manufacturing a material continuously instead of in batches is clear. The inputs and throughputs to continuous manufacturing processes are usually webs. A web is defined as a long, thin, flexible material with negligible bending stiffness about two of its three axes.

Major classes of web materials include film, foil, food, paper, nonwovens, rubber, textiles, and composites of these. Materials range from centimeter-thick metals to micron-thick plastics, widths range from single thin strands to more than 10 m, and line speeds range to more than 2500 m/min. The goal of web handling is getting a web through a machine as fast as possible with minimum damage and waste, while preserving the web's properties.

Academic rigor and the best practices of industry need to be merged for innovation to occur and result in tangible advances.

Web manufacturing forms the raw-material web (e.g., paper making, film extrusion, textile spinning), while web converting (e.g., coating, laminating, printing, sheeting) takes one or more web materials and permanently alters them in some fashion either by changing material properties or causing geometrical or physical changes. Web manufacturing and converting are often done by a combination of mostly art (trial and error) and a little bit of science, depending on the industry. All webs follow the same laws of physics—if you know the physics, you know the behavior.

Web handling is an exact science with model-based design rules; all webs behave fundamentally the same way when pulled through a machine under tension. There even exists a wealth of literature and experts (e.g., D.H. Carlson, 3M Corp.; P.R. Pagilla, Oklahoma State University; and M.D. Weaver, Rockwell Automation) in this area. Monitoring and controlling web velocity and tension is a common web-handling challenge.

The use of a model-based design approach, rather than a trial-and-error design approach, is fundamental in modern mechatronic system design. Why is this approach not more widespread when applied to webs? There is a gap, and time lag, between the academic/research world and the world of industrial practice. In December 2009, Dennis Bernstein wrote an article in the *IEEE Control Systems Magazine* entitled "On Bridging the Theory/Practice Gap." It was timely then and even more so now. In the article, Bernstein explains that both sides contribute to the problem.

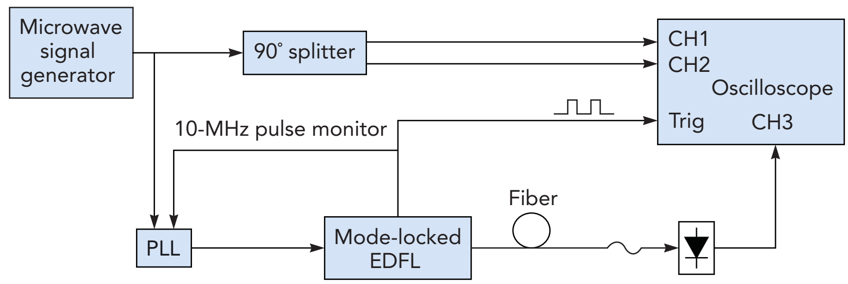
So what needs to happen to bridge this gap? Academic rigor and the best practices of industry need to be merged in an understandable, usable way for innovation to occur and result in tangible advances. On the academic side, professors need to get out of their comfort zone and make each course—from freshman year through the graduate programs—not just a textbook course but an up-to-date fusing of academic rigor and best industrial practice with actual industry case studies as examples. Too hard, too challenging? This is what transformational engineering education is all about.

On the industrial side, companies need to recognize that their competitive advantage comes from an inspired, educated workforce, and that should be their primary concern. Too often, the training budget is the first to be cut with the view that technological advances somehow arrive with the morning newspaper. Too harsh an assessment? I do not think so, and I do not believe the rest of the world thinks so, either. T&MW

OSCILLOSCOPES

Reduce time-base errors in sampling oscilloscopes

Sampling oscilloscopes are often used to measure jitter in gigahertz-rate optical signals. With bit rates that high, errors in an oscilloscope's time base can add jitter to a viewed signal. Engineers at NIST (National Institute of Standards and Technology) have developed a calibration technique that reduces oscilloscope time-base jitter (Ref. 1). Experiments show that the technique reduced time-base jitter from 0.81 ps to 0.22 ps, a factor of nearly 4.



A phase-locked loop locks a microwave signal generator to an erbium-doped fiber laser, which produces an oscilloscope trigger signal.

The test setup in the **figure** uses a microwave signal generator set to 5 GHz. A PLL (phase-locked loop) locks a mode-locked EDFL (erbium-doped fiber laser), which produces optical pulses, to the generator's output.

A 10-MHz feedback signal from the EDFL returns to the PLL to maintain phase lock and to trigger the oscilloscope. The 1550-nm optical beam from the EDFL provides short optical pulses to the photodiode that is connected to the oscilloscope for measurement and calibration.

The signal generator's output also goes to a 90° phase splitter. It produces two sine waves in quadrature that become reference signals for two of the oscilloscope's channels.

The calibration technique uses software developed at NIST that corrects for random and systematic time-base errors. This technique also works on oscilloscopes with an optical input.

Martin Rowe, Senior Technical Editor

REFERENCE

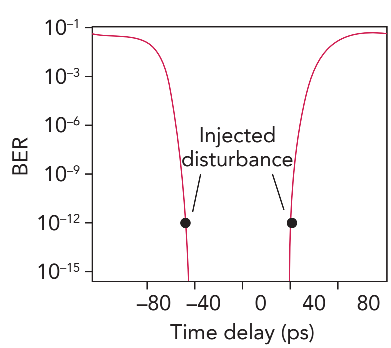
1. Jargon, J., et al., "Correcting Sampling Oscilloscope Timebase Errors With a Passively Mode-Locked Laser Phase Locked to a Microwave Oscillator." *IEEE Transactions on Instrumentation and Measurement,* April 2010. www.eeel.nist.gov/publications/get_pdf.cgi?pub_id=900876.

COMMUNICATIONS TEST

The stressed eye's crest factor

When you think of crest factor, you probably think of AC mains voltage, not serial data streams. Crest factor, defined as V_{PEAK}/V_{RMS}, applies to any AC signal, including the modulating signal that causes sinusoidal jitter. "A New Method for Receiver Tolerance Testing Using Crest Factor Emulation (CFE)," a paper presented at DesignCon 2010 by Ransom Stephens of Ransom's Notes and John Calvin of Tektronix, explains how to apply high crest factor to a data stream. The paper explains how you can stress a receiver under worst-case conditions and measure BER (bit-error rate).

Using an arbitrary waveform generator, you can apply low-probability, high-amplitude jitter at known points in a serial data stream. The problem of accurately measuring BER at 10^{-12} or 10^{-15} is that the test time required to properly evaluate the full effects of random events can range from 30 min to many days. High-amplitude jitter can occur at any time, so if you can apply jitter at sensitive points, you can cut measurement time and increase repeatability in your measurements. The CFE measurement technique can reduce test time to less than 1 min and is 100% deterministic in its ability to be reproduced from run to run.



Applying a high-crest-factor disturbance to a serial data stream lets you verify if a receiver can meet a 10^{-12} BER requirement.

To perform the BER measurement, apply a high-amplitude jitter signal to a bit transition where both the median ISI (intersymbol interference) and half the amplitude of the sinusoidal jitter specified in a serial-data standard occur. If the receiver fails to correctly identify the bit (BER > 10^{-12}), then you can repeat the test and verify if the error is indeed caused by the receiver. You'll know if the failure was caused by ISI, periodic jitter, or random jitter.

You can download the paper and the slides used at DesignCon from the online version of this article (www.tmworld.com/2010_06).

Martin Rowe, Senior Technical Editor

Test ideas

Measurement tips from readers

Helmet tester verifies compliance

A USB data-acquisition module collects accelerometer data to evaluate the impact of a helmet crash.

By Aniket, Consultant for Aum ElectroTech, Mumbai, India

Helmets are designed to minimize or prevent injury in a variety of activities, and they must be tested to ensure they meet industry standards for withstanding impacts. My company has developed a test system that evaluates a helmet's impact attenuation by releasing the helmet from a specific height in guided free fall on an impact anvil. An accelerometer ('g' sensor) measures the force that would be transmitted through the helmet to the wearer's head and compares it to specified performance limits. A LabView application running on a standard PC controls the tester. Although this tester uses a USB data-acquisition module, it could also work with a PCI card in the PC or with a PXI card in a chassis.

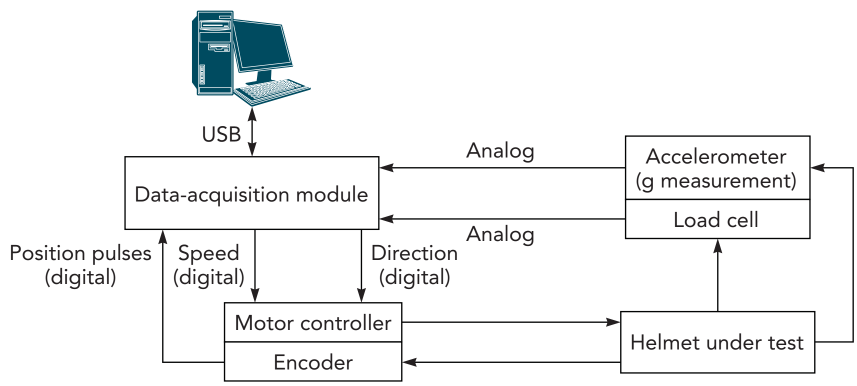


Figure 2. An automated test system measures the g force on a helmet under test.

The impact test system has a firm pedestal, a linear bearing rail, a lift carriage, a drop carriage, and a digitally controlled Panasonic servo motor to lift either the striker or the helmet, depending on the test. **Figure 1** shows the helmet in a stationary position with the striker able to move as required. The test operator positions the striker, which is mounted to the drop carriage, and programs the desired drop velocity. The drop carriage automatically lifts to a height corresponding to the desired impact velocity. The drop tower complies with the helmet-test standards specified by numerous standards bodies.

Figure 2 shows how the test instrumentation connects to the sensors and the helmet. The data-acquisition module uses its digital-output lines to set the motor's direction so it raises or lowers the striker or helmet, while another digital output controls the motor's speed. An encoder senses position markers on the shaft and transmits pulses to a digital-input line, which tracks the anvil's location relative to a starting location.

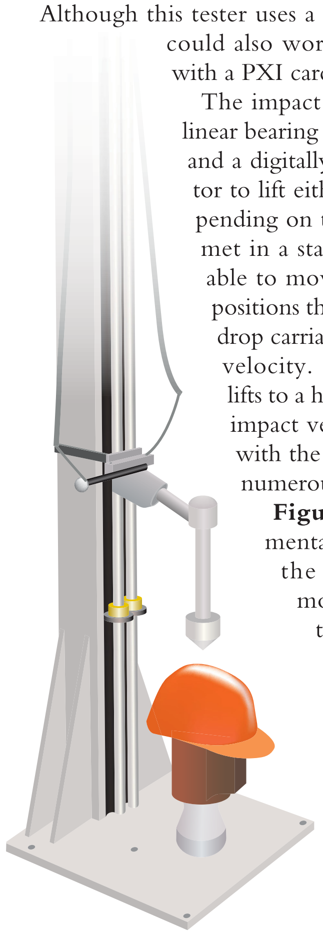


Figure 1. In this configuration, an impactor drops onto a helmet, where sensors record speed, impact attenuation, and other parameters.

A test operator enters information about the helmet size, conditioning environments, and test standard into the system. Test screens that are specific to the test apparatus, standards, and routines let operators perform pre- and post-test instrument verification; then, the system performs the entire test sequence on a helmet.

The results from each test are instantly displayed both numerically and graphically by the LabView application, which also saves the data to a database for later review. (The LabView Database Connectivity Toolkit simplifies record keeping.) When testing is complete, the LabView Report Generation Toolkit produces a test report (including a PDF version); it can also send the report by e-mail to a specified recipient. Test-result documentation includes impact attenuation, retention elongation, helmet stability, penetration resistance, mass, center of gravity, and moment of inertia. The online version of this article contains an additional figure that shows the user interface (www.tmworld.com/2010_06). T&MW

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Electronic *sleuths*

Engineers at Chipworks peer inside integrated circuits and the products they populate in order to perform competitive analysis and look for patent infringement.

BY RICK NELSON, EDITOR IN CHIEF

Want to know what's inside an iPad? Better yet, do you want to know what's inside the chips inside the iPad? The engineers at Chipworks make it their business to find out. They'll tear down electronics devices like mobile phones and reverse-engineer ICs, deriving complete schematic diagrams in order to develop competitive intelligence. With the Chipworks team's help, clients can keep track of what their competitors are doing and look for instances of patent infringement.

The Apple iPad has been in the news lately, and the Chipworks investigation into that device provides a snapshot of Chipworks' capabilities. For example, by noon April 4—one day after the product hit the streets—the folks at Chipworks had surmised that Apple focused on industrial design and usability while employing conservative, low-cost technology under the hood.

Some specifics that Chipworks found: Apple is not using the Texas Instruments do-all touch-screen controller that it used in the iPhone 3G but instead is using the three-chip solution seen in the iPhone 2G; 16 Gbytes of memory are provided by two Samsung K9LCG08U1M 8-Gbyte MLC NAND flash memory chips; the Apple A4 processor is packaged just like the Apple iPhone processors, using package-on-package technology (with the two DRAM die confirmed to be Samsung 128-

Randy Torrance (left), who leads the circuit-analysis team for Chipworks' technical intelligence group, and Sinjin Dixon-Warren, manager of the process-analysis group, reverse-engineer chips to gather manufacturing process data and to extract schematics.

TONY FOUHSE

Mbyte devices); and STMicroelectronics captured the accelerometer design win.

At this point, the iPad seems to be a big iPod instead of a little laptop. As Dick James, Chipworks senior technology analyst, put it, "Essentially, the iPad is an iPod Touch with an enhanced display and much increased battery life. The iPhone 2G-style touch-screen architecture perhaps reflects the date of design start, and we will likely see TI get the design win in the next-generation iPad—especially as we have seen the same [TI] chip in the latest iPhone, iPod Touch, and Magic Mouse."

Of course, many organizations perform teardowns, as do the editors of sibling publication *EDN* in that magazine's Prying Eyes section (www.edn.com/pryingeyes). Where Chipworks stands apart is in its investigations of the ICs inside the products being torn down. Figure 1, for example, show details of the Apple A4 processor inside the iPad: Figure 1a shows a cross section of the device, Figure 1b shows transistor details, and Figure 1c shows the layout.

From MEMS to RF power amplifiers

The hype surrounding Apple's iPad introduction and curiosity about the product is in part why Chipworks decided to tear one down and reverse-engineer the A4. But Chipworks' interests and capabilities extend well beyond teardowns of hot consumer products, reaching to the reverse engineering of various ICs. Chipworks engineers writing in *EDN*'s "IC Insider" section have described the reverse engineering of battery-charger ICs, self-powering RFID devices, LED drivers, CMOS RF power amplifiers, MEMS-based inertial sensors, and DDR SDRAMs.

Writing in a recent "IC Insider" column, Dick James and Randy Torrance, who leads the circuit-analysis team for Chipworks' technical intelligence group, elaborated on reverse engineering: "In the semiconductor industry, RE has long been a recognized and well used part of competitive intelligence. It's commonly leveraged to both benchmark products and support patent licensing activities.... Advances in semiconductor technology, specifically the massive integration of billions of individual devices and masses of func-

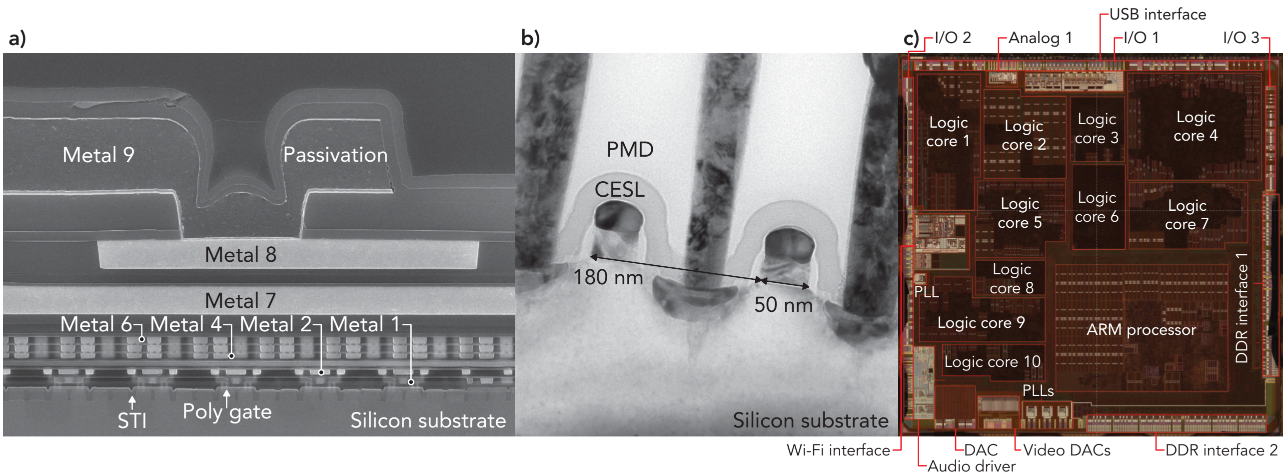


FIGURE 1. Cross-sectional analysis can help investigate processes used to produce ICs such as the Apple A4 used in the iPad, showing (a) metal layers and (b) transistor details. Delayering coupled with the imaging of each layer can derive (c) the circuit layout. Courtesy of Chipworks.

tions into single components, have caused RE to evolve from skunk-works projects in the failure-analysis lab into a specialized niche of the engineering profession." (Ref. 1.)

De-potting the die without damage

To learn more about Chipworks, I spoke with Torrance as well as with Chipworks engineers Sinjin Dixon-Warren, Neal Stansby, and Darko Veselinovic. Reverse engineering typically begins with what Stansby called a "front-end" operation.

Stansby, manager of the Chipworks research and development group, explained, "We have a piece of silicon or possibly multiple pieces of silicon that are buried inside a package, and we've got to get them out without damaging them." He described various techniques for doing that: "If it's a plastic package, you throw it in a beaker of acid and you are done. If it's a ceramic package or a metal package, it can be considerably more challenging and time consuming. We have a recipe book of techniques and different types of equipment that we use to get the actual die out of the package without damaging it."

Process work involves cross-sectional analysis, while circuit reverse engineering centers on imaging layers.

With the die out of the package, the circuit reverse engineering moves on to sequentially exposing the interconnect layers, the device layer, and the substrate. Said Stansby, "We sequentially expose each of the interconnect layers and finally the device layer in a way that reveals the features without damaging them. The challenge we face is that the features are continuously getting smaller and smaller and consequently more and more delicate. Chips are generally getting bigger as well in a lot of cases. If we are trying to expose all of metal 7 on a 12-metal chip, our delayering has to be extremely planar—otherwise, we'll be looking at metal 7 in one area and metal 6 or metal 8 in others." He explained that Chipworks uses a combination of mechanical polishing and wet and dry etching, depending on the materials used in the construction of the chip—such as copper or aluminum interconnect and regular dielectric or low-k dielectric.

Deriving the right delayering recipe can be particularly difficult for devices from new foundries or devices implemented in process nodes the Chipworks engineers haven't dealt with before. And Stansby added that experience with a similar part is no guarantee of quick success, noting, "You might think if I was working on a 130-nm TSMC chip last week and have another this week, they ought to behave the same during the delayering process, but that's not necessarily true. Characteristics such as the density of the wiring on a particular layer can affect the rate at which it etches or polishes off. Or perhaps this week's chip was built with some design-rule waivers to meet some particular design goal." Fortunately, the Chipworks process-analysis group can help.

Process analysis

Process analysis is the domain of Sinjin Dixon-Warren, manager of the process-analysis group of Chipworks' technical intelligence business unit, which relies on cross-sectional analysis to investigate process details. "We like to joke that all Sinjin does is look at cross sections and all I do is take planar looks at layers," said Torrance, adding that, indeed, much process work is done via cross-sectional analysis, while Torrance's work centers on imaging and analyzing layers.

Dixon-Warren said his group does primarily CTI (competitive technical intelligence) analysis, and it also supports the intellectual property group that looks for infringement of patents relating, for instance, to structural features such as the way a via is connected to a metal line or the way a transistor is built. The group can also look for process-oriented

patents that describe a method of manufacturing something. Infringement of such patents can be difficult to prove, because a similar final structure could result from vastly different manufacturing processes. Nevertheless, Dixon-Warren said that Chipworks' investigations, while focused on CTI, can prompt further negotiation or litigation.

A side benefit of Dixon-Warren's team's effort is that the information it gleans can be helpful in determining the optimum recipe for delayering. Stansby said the process-analysis team, for instance, might determine that the top two metal layers are three microns thick and the remaining ones are one micron thick—information that can help the Chipworks engineers calculate optimum etch times and polishing times.

Microscopes are key tools for the Chipworks engineers. Said Stansby, "Any type of microscope you can think of we probably use from time to time." Optical microscopes can help locate interesting features to investigate further in cross section. SEMs (scanning electron microscopes) provide more magnification, and TEMs (transmission electron microscopes), said Stansby, "take you down to close to the atomic level—providing probably the highest magnification that will ever be feasible." Chipworks also makes use of scanning capacitance microscopy, a form of atomic force microscopy that is particularly sensitive to silicon dopant types. Noted Stansby, "It's quite a powerful reverse-engineering technique that allows you to see doped areas of the silicon with pretty good spatial resolution."

A mosaic of images

When undertaking to reverse-engineer a chip, Chipworks tries to have available one sample per layer. Said Stansby, "For a five-metal device, we would have seven layers—the five metals plus the poly diffusion layer where we see the actual transistors and the substrate where we can distinguish the p and n devices."

Once the delayering lab has succeeded in getting a layer exposed, the next step is to image it, and that's difficult for two reasons, said Stansby. First, as the features get smaller, the magnification has to go higher and higher in order to resolve the features of interest.

"For any microscope that we can buy at the magnifications we need, the field of view is just a tiny, tiny, tiny fraction of a percentage of the area of interest," Stansby said. "So, we solve that problem by shooting a two-dimensional mosaic of each layer with slightly overlapping images, and we then have to put those together in a way that is equivalent to one large image." He said it's not uncommon to shoot 60,000 images for each layer of the three to 13 layers a device under investigation might present.

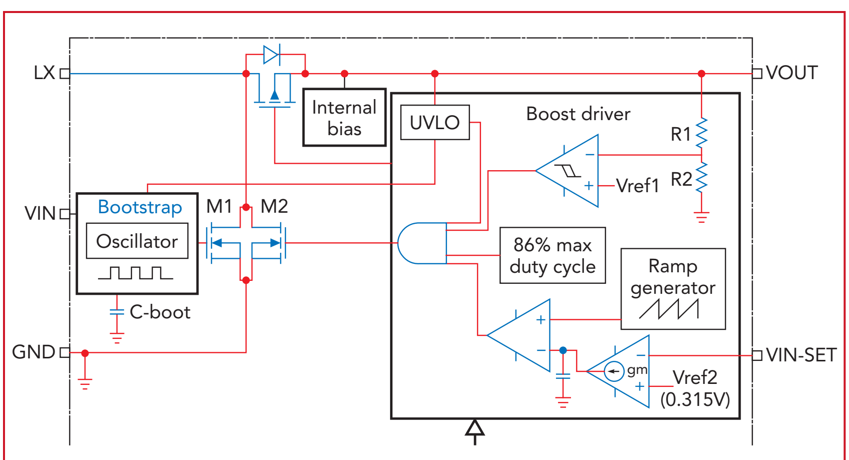


FIGURE 2. Chipworks engineers can glean much information about a chip, enabling them to derive schematics. Shown here is the partial block diagram illustrating a bootstrap circuit oscillator and boost driver of Freescale Semiconductor's SMARTMOS 10 DC/DC converter.

Taking all those images could be very time consuming. SEMs in general, Stansby said, are designed for analytical laboratory use, while Chipworks is trying to push them into something approaching high-volume production use. The company uses commercial SEMs, he said, but they are heavily modified to meet Chipworks' throughput requirements.

Precision and accuracy are also critical, Stansby explained. "Think about what we are going to do with that big beautiful composite image of metal 6; we are going to overlay it over the image of metal 5, and we want to do that with sufficient precision that we can trace a connection that goes through a via" between the two layers. He added, "At a wire pitch of 200 nm or 300 nm, your tolerance of error is about 100 nm over an area of interest that could be 5, 8, or maybe 10 mm wide. Percentage-wise, these things have to be insanely accurate and distortion free in order to trace connections unambiguously." So, in addition to requiring enhancements for throughput, he said, "the SEMs must be optimized for extreme accuracy to keep everything on a very honest coordinate system."

Software eases interpretation

The Chipworks software that ties all the images together and aligns all the layers is called ICWorks. With ICWorks, a user on a CAD workstation can examine all the layers, zooming in and out and popping up and down between layers to view all the vias. The view, said Torrance, is quite similar to what a design engineer or a layout engineer would see, except the ICWorks user is looking at a real image—not the beautifully rectangular graphics of a CAD layout tool.

At that point, Chipworks engineers annotate overtop of the images, identifying all the devices and all the wires. With annotation complete, the ICWorks tool automatically exports a schematic. "Unfortunately, said Torrance, "the schematic it exports is one big monstrous flat schematic" that could be nearly incomprehensible to the average chip designer. Fortunately, he added, Chipworks has on hand engineers "who can create some hierarchy and put together a set of schematics that another engineer could read and understand."

Referring to Chipworks' clients, Torrance said, "At that point, we send you the ICWorks tool, and with the ICWorks tool, you get all the images, you get all the annotation we've done, and you get all the schematics we've done. ICWorks allows you to cross-probe between all of these things so you can select one of the devices in the schematics and then quickly cross-probe over and take a look at the images of it in all the different layers and see how it was built."

System-level microsurgery

While microscopy is the primary tool of process analysis and schematic extraction, electrical test can come into play with system-level nondestructive teardowns. Explained systems engineer Darko Veselinovic, "On some projects, we combine teardowns with performing microsurgery on a die that is still functional," probing signals of interest that have been located through the layer-imaging and schematic-extraction processes. The die being monitored may be on its original PCB (printed-circuit board) or on a test jig built for the purpose.

Veselinovic pointed out some of the challenges of capturing signals of a system under investigation: "Take an automotive application, for example. If we can somehow operate the vehicle in a stationary manner so we don't have to drive it around, that makes it a little bit easier. We can create some extension cables that allow us to locate a controller box in such a position that we can easily reach the signals of interest."

Neal Stansby (seated), manager of the Chipworks research and development group, and Darko Veselinovic, systems engineer, prepare to examine an iPad.

TONY FOUHSE

In other cases, though, a mechanical linkage between controller and vehicle may make that impossible. In that case, said Veselinovic, "We try to open up the case without damaging anything, and then we maybe have to drill a hole in the one part of the case where we can put our probes through. Then, we try to reassemble everything so it's functional and the case is not much bigger than its original size, and we try to put it back in the original position."

With the system operational, it can be operated with external test-and-measurement equipment monitoring the signals of interest. Sometimes, said Veselinovic, the monitoring requires that his team build an FPGA front end, for example, to transport signals of interest though a noisy environment or to enable the transmission of a lot of information over long distances. He noted that Chipworks will take advantage of any access the original designer provided, such as a JTAG port.

Philosophy of reverse engineering

Torrance said he's had the opportunity to speak about reverse engineering at a variety of venues, including meetings of local IEEE chapters, and he said a question he often gets is, "Is this legal?" Indeed it is. Torrance explained that in the US, the Semiconductor Chip Protection Act protects reverse engineering, allowing the technique "for the purpose of teaching, analyzing, or evaluating the concepts or techniques embodied in the mask work or circuitry." Similar legislation, he said, exists in Japan, the European Union, and other jurisdictions.

Torrance said he has also found that "…a lot of people out there just don't seem to know this is possible—that you can take a layer at a time off of a chip and actually image it and see everything. I think a lot of people designing a chip think once they put a package around it, no one will be able to see what's inside, which is not true."

There have been efforts to thwart the investigation of reverse-engineering teams. Said Stansby, "If you scan the world of patents, you'll find all kinds of people patenting manufacturing techniques to try and make it hard to reverse-engineer circuits—for example, structures that look like vias but don't quite make a connection. But the reality is, I don't believe in the history of the company we have ever actually run into any of those in real chips—at least not commercial chips."

Added Torrance, "Occasionally, we'll find a layer with a metal plate, which seems totally useless functionally, with some circuitry underneath it. The only thing we can dream up is that [the designers] are trying to hide the circuits from prying eyes, but that doesn't slow us down much at all." T&MW

REFERENCE

1. Torrance, Randy, and Dick James, "IC reverse engineering—a design team perspective," *EDN*, March 11, 2010. www.edn.com/icinsider.

BOOST CURRENT for high-power tests

BY DAVID WYBAN, KEITHLEY INSTRUMENTS

You can combine voltage and current sources to produce current that exceeds 100 A.

Characterizing solar cells, power-management devices, high-brightness LEDs, and RF power transistors often requires tens of amperes, but power MOSFETs and IGBTs (insulated gate bipolar transistors), can require currents in excess of 100 A. Most power supplies, however, can't provide that much current. Fortunately, you can combine voltage and current sources to achieve higher current than one source can provide.

You can use multiple DC current sources to achieve higher current, but high DC currents will cause the DUT (device under test) to heat, which will increase its resistance and possibly lead to measurement errors. To keep the device cool, you can provide pulsed power to the DUT. Pulsed-current-voltage (I-V) testing is often essential for testing power devices (MOSFETs or IGBTs) and high-power RF amplifiers. Although DC current sources typically don't let you pulse their outputs, you can build pulse circuits yourself or use an SMU (source-measure unit) to generate the necessary pulsed power.

Pulsed-power tests sidestep the problem created by high-power CW (continuous wave) testing. During high-power CW tests, semiconductor material will dissipate the applied power as heat. As the device heats, its conduction current decreases, because its carriers have more collisions with the vibrating lattice (phonon scattering). The self-heating will cause a low measured current. Given that power MOSFETs and IGBTs typically run in pulsed mode—intermittently rather than continuously—testing with low DC-measured currents won't accurately reflect their performance.

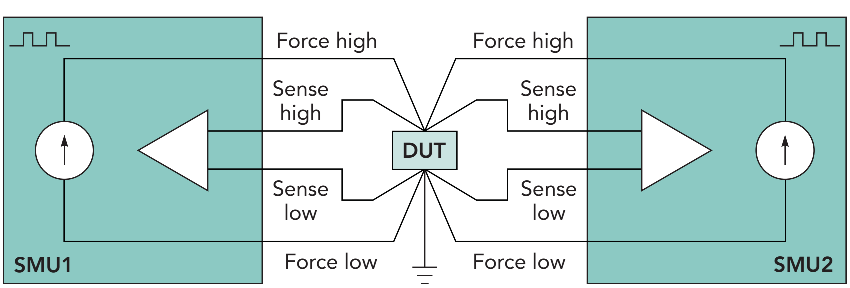


FIGURE 1. Two pulsed-current sources add to each other when connected to the same node.

Pulsed sweeps, where power to a DUT may increase with each pulse, have little impact on many test results, yet they do have some limitations. Pulsed sweeps can affect DUTs such as capacitors, so the results of capacitor tests performed with pulses may not correlate adequately with DC sweeps. Large displacement currents, which can occur at the sharp edges of a voltage pulse, may change the device's electrical properties.

When making a pulsed sweep, you must take pulse width into account. The current pulse must be wide enough to allow sufficient time for the device transients, cabling, and other interface circuits to settle so the system can make a stable, repeatable measurement. But the pulse can't be so wide that it exceeds the test instrument's maximum pulse width and duty cycle limits, which would violate the instrument's allowed power duty cycle. Pulses that are too wide can also create the same device self-heating problems that can occur with DC sweeps.

Combining channels

The most common way to combine SMU channels to achieve higher DC currents is to connect the current sources in parallel across the DUT. The test setup in **Figure 1** takes advantage of Kirchhoff's current law, which states that when you connect two or more current sources in parallel to the same circuit node, their currents will add. Both SMUs in Figure 1 can source current and measure voltage. All of the low-impedance terminals (force and sense) of both SMUs are tied to ground. **Table 1** provides an overview of the characteristics of this particular configuration.

Cabling and test-fixture considerations

When using an SMU for pulsed-power tests, you must configure your cabling and connections in a way that minimizes resistance, capacitance, and inductance between the DUT and SMU. To minimize resistance, use heavy-gauge wire wherever possible, particularly between the power sources and the test fixture. The gauge required will depend on the level of current.

Cabling that must carry 40 A, for example, needs 12-gauge wire. For guidance on choosing cabling for higher current levels, refer to wire-gauge tables such as the one available at www.powerstream.com/Wire_Size.htm. Check the "Maximum amps for chassis wiring" column in the table to find the wire gauge needed to carry the level of current you need.

Low-resistance cabling is critical to preventing instrument damage. Choose cables with resistances of 30 mΩ/m or less for 10-A pulses. Heavy, low-resistance cables will minimize voltage drops between current sources and DUTs.

Keep cable lengths as short as possible, and always use low-inductance cables (such as twisted-pair or low-impedance coax types). Check the SMU's voltage output headroom specification for details on the maximum voltage drop allowed between the source and sense leads. Divide this spec by the desired output current level to get the maximum resistance allowed in your cabling.

Although many believe guarding can minimize the effects of cable charging, this is typically more of a concern for high-voltage testing than for high-current testing. Keep four-wire Kelvin connections as close to the DUT as possible; every millimeter makes a difference.

You should use an SMU's readback capability to measure voltage. For best results, always use the measurement function that corresponds to your source. The current-sourcing SMU voltage readings may vary because of the connections, and the measurement may differ from what reaches the DUT.

Use high-quality jacks on your test fixture. For example, some red jacks contain high amounts of ferrous material to produce the red coloring, which can lead to unacceptably high levels of leakage due to conduction. The resistance between the plugs to the case should be as high as possible, always more than 10^{10} Ω.

Many published test setups recommend adding a resistor between the SMU and the gate pin when testing a FET or an IGBT. These devices tend to oscillate when you apply large amounts of pulsed current through them. Inserting a resistor on the gate will dampen these oscillations and stabilize your measurements. Because the gate draws little current, the resistor won't cause a significant voltage drop.

If your tests require voltages in excess of 40 V, then you need interlocks on the test fixture and SMUs. Install and operate the interlocks in accordance with normal safety procedures.

Ensuring operator safety

Many electrical test systems or instruments are capable of measuring or sourcing hazardous voltage and power levels. It's also possible, under single fault conditions (such as a programming error or an instrument failure), to output hazardous levels even when the system indicates no hazard is present. These high levels make it essential to protect operators from any of these hazards at all times. To ensure operator safety, take these steps:

- Verify the operation of the test setup carefully before it is put into service.
- Design test fixtures to prevent operator contact with any hazardous circuit.
- Make sure the DUT is fully enclosed to protect the operator from any flying debris.
- Double insulate all electrical connections that an operator could touch. Double insulation ensures the operator is still protected, even if one insulation layer fails.
- Use high-reliability, fail-safe interlock switches to disconnect power sources when a test fixture cover is opened.
- Where possible, use automated handlers so operators do not require access to the inside of the test fixture or have a need to open guards.
- Provide proper training to all users of the system so they understand all potential hazards and know how to protect themselves from injury.

It's the responsibility of the test-system designers, integrators, and installers to make sure operator and maintenance personnel protection is in place and effective.—*David Wyban*

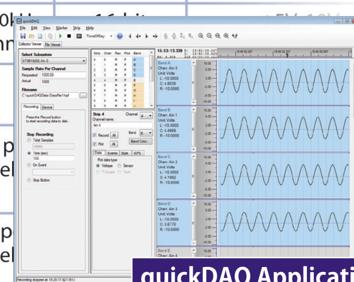
Performance Without Compromise

...USB Data Acquisition

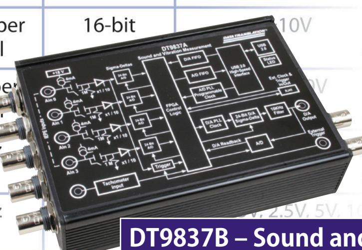
Product Selection Chart

			Analog Input Features			
	Model	**Summary**	**# of Channels**	**Throughput**	**Resolution**	**Input Range**
High Res.	DT9824	**ISO-Channel™**, High Stability, High Accuracy, Fully Isolated USB Data Acquisition Module	4DI	4800Hz per channel	24-bit	±312.5mV, ±625m ±1.25V, ±10V
Low Cost	DT9810	Lowest cost, 10-bit, non-isolated	8SE	25kHz		
	DT9812-2.5V	Low cost, 8 analog inputs, 12-bit, 2.5V range, non-isolated	8SE	50kHz		
	DT9812-10V DT9813-10V DT9814-10V	Low cost, up to 24 analog inputs, 12-bit, 10V range, non-isolated	8/16/24SE	50kHz	12-b	
	DT9816 DT9816-A	Low cost, simultaneous, 6 A/Ds @ up to 150kHz, 16-bit, non-isolated	6SE	50kHz/150k per chann		
	DT9853 DT9854	Low cost, up to 8 analog outputs, 16-bit, 16 digital I/O, 1 C/T, 300V isolation	–	–		
Sound & Vibration	DT9837 DT9837A DT9837B	4 IEPE (ICP) sensor inputs, tachometer, simultaneous A/Ds	4 IEPE (SE) + 1 Tacho	52.7kHz p channel		
	DT9841-VIB	8 IEPE (ICP) sensor inputs, simultaneous A/Ds with DSP, 500V isolation	8 IEPE (SE)	100kHz p channel		
Simultaneous High Speed	DT9832A	Simultaneous, 2 A/Ds @ 2.0MHz each, 500V isolation	2SE	2.0MHz per channel	16-bit	
	DT9832	Simultaneous, 4 A/Ds @ 1.25MHz each, 500V isolation	4SE	1.25MHz per channel	16-bit	10V
	DT9836	Simultaneous, up to 12 A/Ds @ 225kHz each, 500V isolation	6 or 12SE	225kHz pe chann		
High Speed	DT9834	High-speed, up to 16 analog inputs, 500kHz, 16-bit, 500V isolation	16SE/8DI	500kHz		
	DT9834-32	High-speed, up to 32 analog inputs, 500kHz, 16-bit, 500V isolation	32SE/16DI	500kHz		V, 2.5V, 5V, 1
Temp.	TEMPpoint	**ISO-Channel™**, Thermocouple, voltage, or RTD inputs, A/D and CJC per input, high accuracy	8-48	10Hz per channel	24-b	

DT9824 – ISO-Channel™, High Resolution



quickDAQ Application Software



DT9837B – Sound and Vibration

DT8837 – Sound and Vibration for Ethernet

Table 1. Characteristics of two current sources in parallel

Characteristic	Definition
DUT current	$I_{DUT} = I_{SMU1} + I_{SMU2}$
DUT voltage	$V_{DUT} = V_{SMU1} = V_{SMU2}$
Maximum source current	$I_{MAX} = I_{MAX\ SMU1} + I_{MAX\ SMU2}$
Maximum voltage	Limited to the maximum voltage capability of the smaller of the two SMUs

To obtain maximum output with this setup, you should set the output currents for both SMUs to the same polarity. Whenever possible, configure one SMU as a fixed source and let the other SMU perform the sweep. During a sweep, the current source's output impedance changes. The DUT's output impedance may also change significantly, such as from a high-resistance off state to a low-resistance on state. Those changing impedances may cause a change in the circuit's overall settling time at each bias point. Although this transient effect dampens, fixing one SMU's source and sweeping the other's usually results in more stable and faster-settling transient measurements, which increase test throughput.

Merging pulse sweeps

Adding current sources when performing a DC power sweep is rather intuitive, but merging pulsed sources is not. Implementing this test method demands extraordinary caution to ensure the safety of test-system operators. You must, for example, provide insulation or install barriers to prevent user contact with live circuits.

Additional protection techniques will prevent damage to the test setup or the DUT. Furthermore, multiple pulses must be tightly synchronized (with nanosecond precision) so the power supply won't apply power to DUTs that are not yet turned on, as this could damage them.

Figure 2 shows the voltage across a high-power precision resistor (0.01 Ω, ±0.25%) that was produced by a single SMU at 10 A for 300 µs and by four SMUs at 40 A for 300 µs. The 10-A pulse, measured with an oscilloscope, shows a waveform of 0.1 V (10 A × 0.01 Ω). The 40-A pulse produced a waveform of 0.4 V magnitude. The 40-A pulse is delayed relative to the 10-A pulse because of the longer rise time needed to achieve that amplitude.

The curves in **Figure 3**—which were taken from a test of a P-N diode—show that DC and pulsed-current sweeps produce identical increases in current. The programmed pulse sweep resulted from a combined four SMUs. Note the correlation of the single-SMU DC sweep up to 3 A, the single-SMU pulse sweep up to 10 A, and the four-SMUs pulse sweep that produces 40 A. This experiment verified the validity of combining four SMU channels and pulsing to achieve 40 A on two-terminal devices (resistor and diode). With certain modifications, this technique is equally valid when applied to testing a three-terminal device, such as a high-power MOSFET.

To maximize accuracy and precision, you can apply several measurement techniques. You can use an SMU's measure functions to read the actual value of the applied voltage. The programmed value may not be the same as the voltage actually applied to the DUT. With multiple SMUs in parallel, the source offsets may add and become quite significant, so you need to measure the actual voltage output, not just the voltage that you've programmed.

By using four-wire (Kelvin) measurements for high-current testing, you can bypass the voltage drop in the test leads. The additional two wires bring high-impedance voltage sense leads to the DUT.

With very little current flowing into the sense leads, the voltage seen by the sense terminals is virtually the same as the voltage developed across the unknown resistance. At 40 A, even a small resistance such as 10 mΩ in the test cable can produce a 0.4-V drop over the length of each test lead. If an SMU forces 1 V at 40 A through a cable with a 10-mΩ resistance, two test leads will result in 20-mΩ resistance. With two-wire measurements, the total voltage drop will be 0.8 V.

Making four-wire measurements will result in significantly better accuracy on both the sourced and measured values. Four-wire measurements eliminate the voltage drop in the current-carrying wires that can affect the measurement. "Cabling and test-fixture considerations," p. 34, explains how to minimize errors and maximize safety when making high-current measurements.

Connecting power sources to DUT nodes

When using multiple power sources, don't use more than one voltage source at each DUT node. Many test sequences use voltage sweeps that force a voltage across a DUT and measure current. In the case where more than one

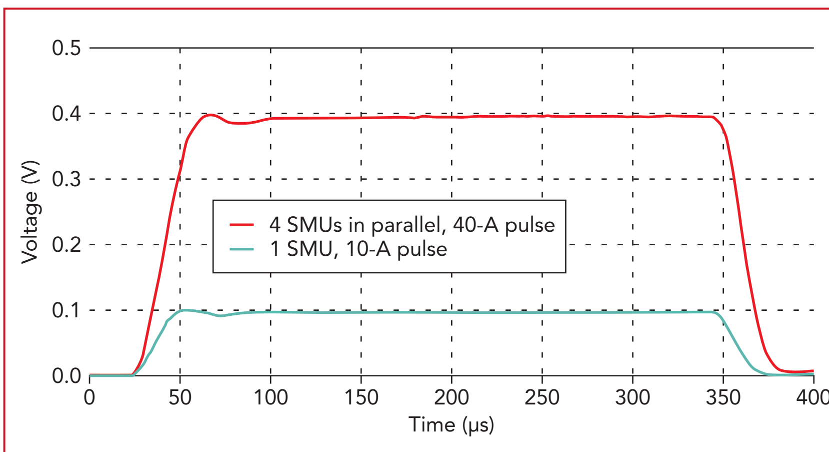


FIGURE 2. Four SMUs, all producing 10 A across a precision load, add currents to produce a 40-A, 300-µs pulse.

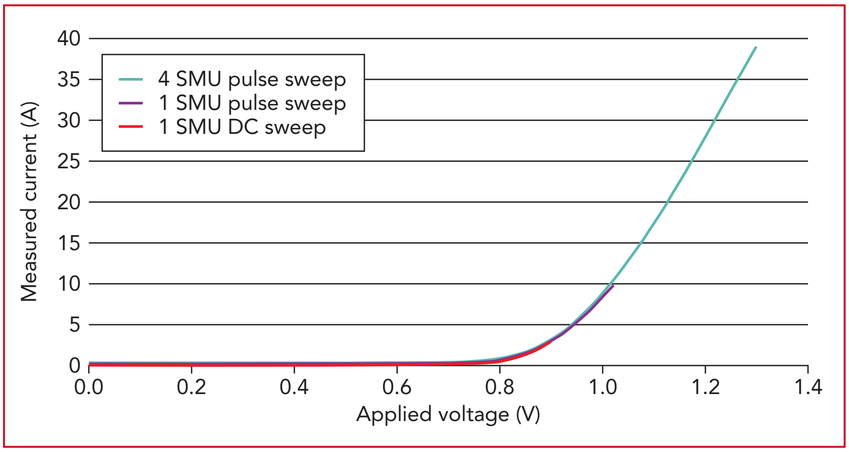


FIGURE 3. Pulsed and DC current sources produce overlaying curves as the current rises.

SMU is connected in parallel to a single terminal of the device, you might decide to set all sources to voltage-source mode and measure the DUT's current. Before you do that, consider these factors:

- A DUT can have a higher impedance than an SMU that is in voltage-source mode. The DUT's impedance can be static or dynamic, changing during the test sequence.
- Even when all SMUs in parallel are programmed to output the same voltage, small variations between SMUs related to the instruments' voltage source accuracy mean that one of the SMU channels will be at a slightly lower voltage (millivolt order of magnitude) than the others.

If you connect three voltage sources in parallel to one terminal of a DUT with each operating at near-maximum current and the DUT is in a high-impedance state, then all current will go to the voltage source that produces the lowest voltage, which will most likely damage that voltage source. If you connect SMUs or other power sources in parallel to a single terminal of a DUT, configure only one to source voltage. The others should source current.

Figure 4 shows incorrect and correct configurations for connecting SMUs in parallel. An incorrect configuration (Figure 4a) could allow high currents to damage the SMU that sources a slightly lower voltage. The configuration in Figure 4b doesn't run the same risk of instrument damage, but it introduces additional error into the measurement that you must account for in the system's error budget. The "hybrid" approach in Figure 4c prevents SMU damage and lets you add current sources as needed to reach the application's current requirements.

When you connect two SMUs with the same output capacity in parallel to a single node in the circuit, one SMU must be able to sink all of the current produced by the other. This condition can occur, for example, when one of the leads breaks contact with the DUT (such as when the lead is accidentally disconnected or a contact isn't made properly). Thus, there will be a short period during which one SMU must sink all the current from the other. The SMU that will be forced to sink current is the one with the lowest voltage or lowest impedance, most likely the one sourcing voltage.

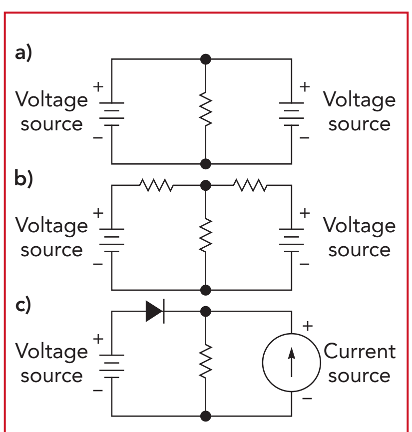


FIGURE 4. (a) Connecting two voltage sources together can result in damage to the lower-voltage source. (b) Resistors reduce the current, and (c) a diode prevents current from entering a voltage source.

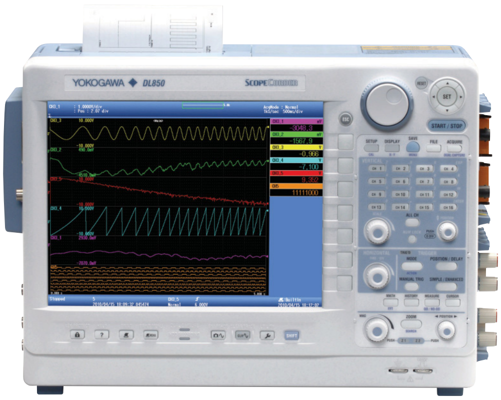
Adding a diode

To protect the signal input of the SMU forcing voltage, you can add a diode such as a 1N5820. A diode offers a much faster response than a fuse and has a much smaller forward voltage drop (typically around 1 V) than a resistor.

To be truly safe when using this method, use a diode to protect all the SMUs in the configuration. If the DUT goes into a high-impedance state, the current sources will try to force their current into the voltage-sourcing SMU, but the diode will prevent that from happening. Without the diode, the current-sourcing SMUs would increase their output voltage until they either forced all their current through the voltage source SMU or they reached their voltage limit. If they reached their voltage limit, the current sources would go into compliance and become voltage sources themselves.

Compliance (such as voltage compliance for a current source) occurs when the output voltage of the current source reaches its voltage limit. The current source "complies" with the voltage limit and becomes a voltage source whose voltage is programmed to the voltage limit. If this happened, you'd have multiple voltage sources in parallel. Even if their voltage limits were set to exactly the same value, their outputs would likely be slightly different and they would damage each other.

Putting a diode on each and every SMU in the configuration in Figure 4c has some consequences. First, adding the diode means that this test setup can only source power but not sink it, because the diodes prevent current from passing into the SMU. Second, to obtain maximum output voltage, you need to use four-wire connections on the current sources around the diode, because the voltage drop across the diode may cause the current sources to reach compliance prematurely. At these current levels, the typical voltage drop across a diode is about 1 V. T&MW



ScopeCorder gets a major upgrade

Yokogawa's DL850 ScopeCorder is the successor to the company's popular DL750, which is found in systems such as automotive, energy, and electromechanical systems. The DL850 features a 10X measurement speed increase to 100 Msamples/s (12 bit), an 8X increase in channel count to 128, a 4X increase in hard-disk capacity to 160 Gbytes, and a 2X increase in acquisition memory to 2 Gbytes.

The modular design of the DL850 is backward-compatible to the DL750, so you can use your existing input modules with the new mainframe. With the DL850, Yokogawa has added the 100-Msamples/s analog input card, a scanner module to get to the 128 channels, and a digital-input card.

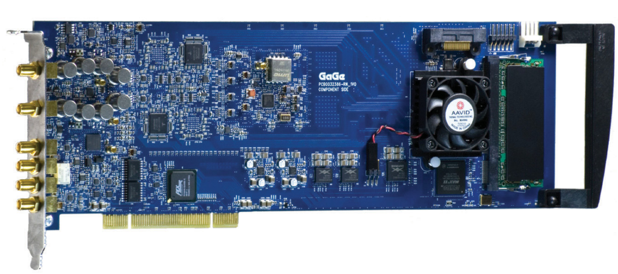
The DL850 adds two new interfaces: an optional SATA interface for attaching an external higher-capacity hard drive and an IRIG interface for attaching a time-synchronization module. There's also an SD card slot that supports up to 16 Gbytes. These go along with the GPIB (optional), Ethernet, and USB ports.

Base prices: mainframes—$6995 (256 Msamples of data memory); input modules—$950 to $3000. *Yokogawa, tmi.yokogawa.com.*

Digitizer goes for signal fidelity

The CS1250X pair of 12-bit digitizers from GaGe emphasize ENOB (effective number of bits) based on the SINAD (signal-to-noise and distortion) measurement method. The PCI cards, which have one channel (CS12501) or two channels (CS12502), can sample at 500 Msamples/s with an analog bandwidth of 350 MHz.

Each card's ENOB reaches 10.1 bits with an input frequency of 10 MHz when operating at the ±500-mV range (other input ranges are ±100 mV and ±2 V). At 200 MHz,



each card has an ENOB of 9.5 bits. Frequency response remains flat over the Nyquist frequency range of 0–250 MHz.

Both models can trigger an acquisition on analog voltage levels or based on an external pulse. For the two-channel CS12502, you can trigger an acquisition on either channel with different voltage levels for each. Trigger levels are software programmable in increments of 0.5% of full scale.

Prices: CS12501—$8495; CS12502—$10,995. *GaGe, www.gage-applied.com.*

PCIe 3.0 tools tackle design, test, debug

Tektronix has released a suite of test products for PCIe (PCI Express) 3.0, spanning protocol to physical analysis in a single platform. The TLA7SA16 and TLA7SA08 logic protocol-analyzer modules, bus-support software, and probes combine to give developers a time-correlated view of system behavior, starting with protocol analysis and working down to the physical layer to debug the root cause of problems.

The logic protocol-analyzer modules provide x8 and x4 lane support, with support for 8.0-GT/s acquisition rates and PCIe link widths from x1 through x16. The modules are compatible with previous-generation PCIe specifications. They dynamically track changes in link width, link speed, and bus power states, and include a trigger state machine that spans all layers of the protocol.

Up to 16-Gbyte-deep memory (for x16 link) increases the chances of capturing both an error and the fault that caused the error. To make maximum use of memory, you can store everything on the bus or use real-time hardware filtering and conditional storage to store selected transactions over an 11-day period.

Tektronix' PCIe 3.0 tester includes a comprehensive selection of probes, including midbus, slot interposer, and solder-down connectors, that support PCIe 3.0 channel lengths up to 24 in. with two connectors, offering minimal electrical loading with high signal fidelity and active equalization to ensure accurate data recovery of closed eyes.

Base price: $60,000. *Tektronix, www.tektronix.com.*

System tests EMC signals up to 6 GHz

The ITS 6006 immunity test system from Teseq lets you perform radiated EMC emissions testing over an extended frequency range of 80 MHz to 6 GHz. Useful for a variety of EMC applications, the system comprises an RF signal generator with AM and PM modulators, RF switches, inputs for up to three external power meters, ports for monitoring and controlling the EUT (equipment under test), amplifier control outputs, and software for comprehensive EMC testing.

Digital inputs and outputs are combined with analog and optical inputs for increased versatility and functionality. Multiple EUTs can be monitored and controlled via the ITS 6006's four TTL outputs and eight inputs, which include two digital inputs with a voltage range of 0 V to 24 V, one analog port, and one optical port.

An integrated RF switch network allows the RF signal generator to be switched to one of up to four power amplifiers. Two additional RF switches can be used to combine two amplifier output paths into a single antenna connection. The ITS 6006 network can be controlled remotely via an RS-232, a LAN, or a USB interface.

Base price: $23,900. *Teseq, www.teseq.com.*

JDSU adds CWDM OSA to multiservices test platform

The T-BERD/MTS-4000 multiple-services test platform from JDSU now includes the COSA-4055 module, a CWDM (coarse wavelength division multiplexing) OSA (optical spectrum analyzer) with a wavelength range of 1260 nm to 1630 nm. New CWDM test capabilities help service providers install, maintain, and upgrade metro/access links and CWDM systems by providing accurate measurements of wavelengths and power levels for CWDM channels, as well as displaying the complete spectrum.

JDSU claims that the COSA-4055 packs the functionality and speed of a conventional OSA in a handheld package at a fraction of the price. One-button auto-testing eliminates the special training typically required to perform CWDM testing. The battery-operated COSA-4055 also provides CWDM testing over the full wavelength range, a complete spectral trace, tabular results, and drift measurements.

JDSU, www.jdsu.com.

Module sports eight isolated inputs

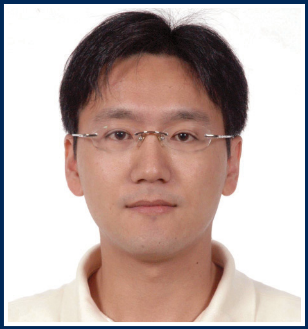
In addition to two 16-bit analog inputs and four solid-state relay outputs capable of switching up to 3 A each, the Pico-II8IDO4A USB 2.0 module from Acces I/O provides eight individually optically isolated inputs. Circuit isolation makes the Pico-II8IDO4A useful in control and instrumentation applications where high-voltage protection is required. The instrument offers individual channel-to-channel isolation, and the two 16-bit analog inputs let you monitor and control a variety of system parameters, such as temperature, voltage, and humidity.

You can use the Pico-II8IDO4A with most USB-supported operating systems. It comes with a free software package that is compatible with Linux (Mac OS X) and Windows 2000/XP/2003/Vista/7 and contains sample programs and source code in Visual Basic, Delphi, and Visual C++ for Windows.

Price: $295. *Acces I/O, www.accesio.com.*

Frame grabbers get Power over Ethernet

By Ann R. Thryft, Contributing Technical Editor



Neil Chen
Product Manager for Vision Products
ADlink Technology

Although cameras equipped with PoE (Power over Ethernet) have appeared in the last couple of years, the interface is new in frame grabbers, according to Neil Chen, product manager for vision products at ADlink Technology. Chen commented on the advantages of using PoE in high-speed, industrial machine-vision systems, and on why customers are asking for PoE-enabled frame grabbers in addition to PoE cameras.

Q: What are PoE's main benefits?
A: All technologies that send power and data over a single cable between cameras and frame grabbers eliminate the power cable and its power brick, saving space, reducing cost, and simplifying installation. PoE's main advantages are cable length, since Ethernet cable carries power and signals up to 100 m, and its lower cost of cabling, because Ethernet cable is relatively inexpensive. A third benefit is the ability to plug in a PoE device without having to restart the computer.

INSIDE THIS REPORT

Q: Are there any disadvantages?
A: The inherent latency in Ethernet communications works against the need of some machine-vision applications for real-time signal speeds. The other main disadvantage is the extra packet overhead needed for the Ethernet protocol, which adds to the system's CPU load. This can affect the high-performance computing needs of some machine-vision systems.

Q: What's the advantage of a PoE frame grabber?
A: Most PCs don't have PoE interfaces. Although PoE routers and switches exist, customers don't want to install a lot of peripheral devices to get this capability. Since most PoE cameras support Ethernet cables and external power cables, it's simpler to connect them to a PoE frame grabber in the PC.

A PoE device automatically detects the system's PoE and non-PoE devices so it can decide whether to send power. For example, if a PoE frame grabber sends power to a non-PoE camera, the camera will crash. Our GIE62+ PoE frame grabber also contains a power-management IC to provide short-circuit, inrush current, and current-limit protection to protect the connection between a PoE frame grabber and a PoE or non-PoE camera.

Q: What can link aggregation do for machine vision?
A: Only a few machine-vision cameras support the Link Aggregation Control Protocol (LACP). In IT networking, LACP is used to aggregate multiple Ethernet links, or ports, to get higher data-transfer speeds than the current Ethernet standard allows for a single link. In high-speed machine-vision systems, doubling GigE Vision's current 1-Gbps data transfer speed in a frame grabber would double frame rates for less than twice the cost.

Although you can theoretically aggregate 10 separate GigE Vision links to get 10 Gbps, right now you can use existing LACP technology to get up to 2 Gbps, such as with the two independent Gigabit Ethernet ports in the GIE62+. The disadvantage is that you also double the number of cables.

Q: What's coming next in peripherals for PoE?
A: Consolidating the number of end devices. This spring, ADlink is releasing an all-in-one, rugged, dedicated, machine-vision PC with independent PoE ports, a multicore processor, hard-disk and solid-state storage, isolated digital input/output lines, and serial communication for high computing power and multi-camera imaging applications, such as 3-D machine vision. □

EDITOR'S NOTE

Inspection gets more diverse, portable

By Ann R. Thryft
Contributing Technical Editor

The variety of inspection system configurations is getting more diverse. As one example, designers of PC-based machine-vision systems are welcoming hot-pluggable technologies such as PoCL (Power over Camera Link) and PoE (Power over Ethernet) to reduce power and cabling, simplify installation, and fit more functionality in less space (p. 43). To these advantages, PoE adds the flexibility of longer cables, although at the price of Ethernet's notorious latency. New PoE-enabled frame grabbers will further cut down the number of interfaces and end devices users must hassle with.

As another example, the GigE Vision spec's latest update makes it possible for the first time to control networked devices other than streaming cameras with the same API (application programming interface), control protocol, and switch, further integrating a larger number of devices, as well as simplifying software (p. 45).

Some inspection systems have become so small that they are portable (p. 46). Desktop AOI (automated optical inspection) systems are replacing in-line AOI machines in some applications as their capabilities become more powerful and sophisticated. And smaller systems are also emerging. Laptop PCs are becoming viable platforms for inspecting small flat panels, and even cellphones can now perform some machine-vision tasks, although not yet at the levels needed for electronics inspection. □

Contact Ann R. Thryft at athryft@earthlink.net.

HIGHLIGHTS

Dual-beam system performs 3-D nanoscale characterization

The Helios NanoLab x50 DualBeam system from FEI combines a high-resolution SEM (scanning electron microscope) with the company's Tomahawk FIB (focused ion beam) to deliver the imaging and milling capability necessary for applications in semiconductor and materials science research and development. The Tomahawk FIB provides SEM and FIB live monitoring of milling operations, a smaller FIB spot for more precise milling control, and higher beam currents for faster material removal on large structures, such as TSVs (through-silicon vias).

The Helios 450(S) series is intended primarily for semiconductor labs working with sub-32-nm nodes and advanced packaging techniques such as TSVs and multi-die stacks. The Helios 650 targets academic and industrial research centers working in advanced material characterization and modification down to a single nanometer scale. It delivers subnanometer resolution at extremely low beam energies to provide surface-specific imaging. www.fei.com.

Trade show to be renamed in 2011

"Automate" will be the new name for the International Robots, Vision & Motion Control Show sponsored by the Robotic Industries Association, the Automated Imaging Association, and the Motion Control Association. The show will be held in Chicago, IL, March 21–24, 2011.

"We're very excited about the new show name because it serves as a call to action for companies in every industry," said Jeffrey A. Burnstein, president of Automation Technologies Council, the umbrella group for the three organizations. "Now is the time for companies to automate so they can take advantage of technologies like robots, vision, and motion to allow them to improve productivity, speed time to market, boost product quality, and lower overall costs." www.machinevisiononline.org.

PCIe frame grabber handles dual composite-video cameras

Based on the PCI Express bus, the PIXCI SV7 frame grabber from Epix digitizes analog video from one or two standard composite-video cameras (NTSC, RS-170, PAL, or CCIR). The two inputs are independent, allowing image capture at different resolutions, frame rates, and video formats. Digitized video is transferred to the PCIe bus at video rate.

As a PCIe bus master, the PIXCI SV7 board transfers image data without using the host computer's processor. Images can be transferred to computer memory at full or reduced frame rates for processing or analysis by the host computer's processor, or they can be transferred to other targets on the PCIe bus.

The frame grabber offers programmable gain, hue, brightness, saturation, and contrast to condition the video signal. In addition to two BNC jacks for the video cameras, the PIXCI SV7 provides SMA connectors for TTL trigger-in and strobe-out functions. Housed in one computer, up to four PIXCI SV7 boards can capture composite video at the same time from up to eight video sources.

The frame grabber comes with XCAP-Lite imaging software. Compatible with Windows 95, 98, ME, NT, 2000, XP, Vista, and 7, as well as Linux, XCAP-Lite provides independent capture and adjust dialogs for each of the two inputs. www.epixinc.com.

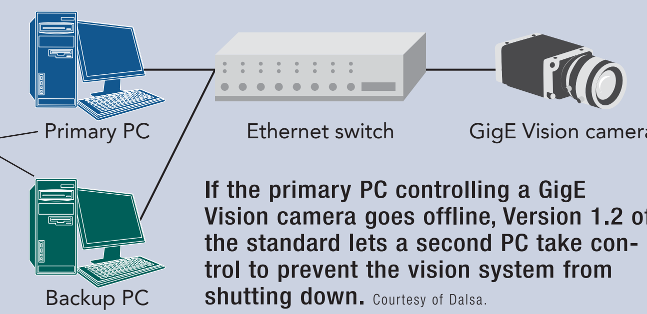
More GigE Vision, Camera Link updates

By Ann R. Thryft, Contributing Technical Editor

More updates are coming in the GigE Vision and Camera Link camera interface standards from the AIA (Automated Imaging Association). In January, the association released GigE Vision version 1.2, which provides several improvements including support for nonstreaming devices. By the end of 2010, the AIA expects to have a draft specification of GigE Vision 2.0, which will include formal support for 10 GigE. The next update to Camera Link will be Camera Link 1.3, which the AIA hopes to release before November; a more thorough revision, Camera Link 2, is just getting underway and is not expected to be completed until 2011.

The main focus of GigE Vision 1.2 is the ability to control GigE Vision-enabled devices other than cameras—in particular nonstreaming devices such as strobe lights—over the same switched network, said Eric Carey, chair of the AIA's GigE Vision standard committee and director of R&D for Dalsa. These devices can be attached to the network with the same switch that connects GigE Vision cameras, and they will be automatically recognized by the network's computers. The ability to control all these devices with a common control protocol will help simplify software development.

"Because of customer feedback we've received from vendors, we also want to increase the robustness of GigE Vision systems," Carey said. "The PC that's connected to a GigE Vision camera can crash or experience other problems that interrupt the application. With version 1.2, logic hooks in the primary application that controls the camera allow a second PC to take control of the camera if the first PC goes offline" (**figure**).



If the primary PC controlling a GigE Vision camera goes offline, Version 1.2 of the standard lets a second PC take control to prevent the vision system from shutting down. Courtesy of Dalsa.

Version 1.2 also includes unconditional streaming. In version 1.0 the camera expects to get a message from the application every few seconds and shuts down the connection if that message stops coming. But in some applications, streaming must continue, Carey said. In version 1.2, this function can be disabled so the camera streams images even if the primary control application has died or the PC has shut down.

At present, the GigE Vision committee is considering five main features for inclusion in version 2.0, said Carey. First is formal support for 10 GigE and link aggregation. Although for practical reasons most GigE Vision 1.0-compliant products do not support link speeds higher than 1 Gbps, version 1.0 does not prevent those higher speeds. The committee will explicitly state this in the 2.0 spec. In addition, version 2.0 will more clearly define how link aggregation can be used for GigE Vision devices.

Next is support for JPEG, JPEG 2000, and H.264 data compression. The third feature, data-flow-control management, prevents congestion when there's a big burst of data. The last two features are a real-time trigger to help synchronize multiple cameras and a frame-packing mechanism for smaller images to reduce packet overhead, in turn reducing the CPU image-processing load.

"We hope to have a draft of GigE Vision 2.0 by the end of this year, but the full specification will probably be ready around the middle of 2011," said Carey. Two minor features for version 2.0 are a generic method of identifying pixel formats and a method for adding new ones, since there are sometimes inconsistencies in how pixel formats are named, plus an appendix containing information that doesn't fit easily anywhere else, such as how to connect GigE Vision devices to the more ruggedized Ethernet cables.

As it prepares the next generation of Camera Link, version 2, the AIA continues to make incremental improvements to the original standard, said Jeff Fryman, the AIA's director of standards development. Camera Link 1.2 included the Power over Camera Link interface and the 26-pin mini-Camera Link connector. "The 1.3 extension, which we hope to finalize prior to November, will include Camera Link Light, a smaller connector with a 14-pin configuration and a different cable, and 'deca,' or 10-tap, mode," he said. This extension will also include electrical design, performance, and test requirements for cables, including an eye-mask and a bit-error-rate test.

Although Camera Link cable has a 10-m nominal distance, it can carry signals more than 10 m at 40 MHz, but less than 10 m at 85 MHz. "Ten years ago, everyone was using 40-MHz or slower cameras, so distance wasn't an issue," he said. "Now we know the cable is too long for faster speeds." □

Desktops make inspection more accessible

By Ann R. Thryft, Contributing Technical Editor

Like most electronic systems, inspection systems have become more compact and more capable as processors and other components have become smaller, faster, and more powerful. A class of inspection systems, called desktops or benchtops, has arisen with smaller footprints and lower costs, yet with most of the capabilities of their larger counterparts. They are often used in labs or other offline locations for testing samples taken from the production line. Now, some EMS (electronic manufacturing services) providers and electronics OEMs are asking for even smaller systems.

There is definitely a trend toward smaller AOI (automated optical inspection) systems in assembled PCB (printed-circuit board) inspection, said Henk Biemans, GM of Marantz Business Electronics. "We developed our first desktop AOI machine in 1996 for internal use in our audio-visual production lines," he said. "We needed something to replace manual inspection, which was done mostly offline for through-hole and surface-mount components, because they had become too small and too many to inspect reliably with the human eye."

Users occasionally want to test their products post-print or post-placement in addition to post-reflow, said Biemans. With a desktop AOI machine or an offline AOI system, they can put in a batch of boards and run them without holding up the production line. This flexibility is especially important for EMS providers, which represent 80% of Marantz' customers for desktop AOI systems.

Desktop machines' prices, at around \$50,000 or so, are about one-quarter to one-third of inline machine prices, making AOI more accessible to smaller companies, Biemans explained. Instead of buying a couple of inline systems, some customers purchase many desktop machines and install them in multiple places around the factory, not only in the surface-mount line.

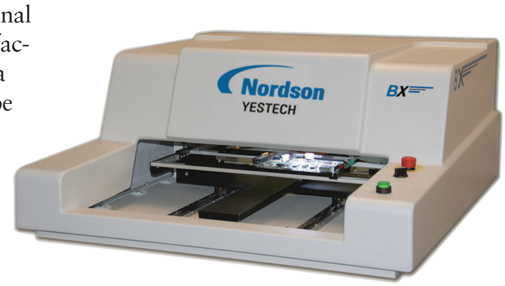
An offline AOI system can be used in conjunction with the Marantz iSpector desktop AOI system (in black, upper left) to eliminate manual handling of PCBs and serve multiple product lines. Courtesy of Marantz.

When desktop AOI systems were new, they were slower than the big inline AOI machines, but they could be programmed more quickly, so they were used for simpler tasks, said Biemans. Large inline AOI machines are usually still faster at top speed, but desktop machines have become almost as powerful, while still being easier to program. And desktop AOI technology is now used for a wider range of applications.

"Because they can be so difficult to program and it takes so much time to get them up and running, inline AOI systems can be line-stoppers," explained Biemans. "If you're an ODM [original design manufacturer] with a huge factory producing a board that takes a couple of months to develop, maybe that's no problem. But in the EMS world, that won't work: You need to run some products in the morning, entirely different ones in the afternoon, and they all have to be inspected and shipped that same day."

Desktop AOI machines cost less than their larger inline cousins because they are less complex, so there's less need for mechanics such as conveyors for manipulating the board, said Don Miller, CEO and president of Nordson YesTech, which manufactures inline and benchtop AOI systems. Benchtops are often used in lower-cost areas where you might not want to place optical inspection inline, and they offer more flexibility because you can also use them to inspect boards throughout the various process steps. "Because of their lower price, benchtop units used to be viewed as less capable, but that's not necessarily the case today," he said. "Our benchtop AOI unit runs the same software as our inline unit, and the programs are interchangeable, so for all practical purposes, it has the same capabilities."

A large inline machine takes up more floor space, can be difficult to move, and may be committed to a production line, said Nordson YesTech's international manager Josh Petras. But a benchtop system can be moved easily from one line to another or from the production floor to a different area for test or failure analysis of the board. Some of the company's EMS customers place its benchtop AOI system next to the production line and emulate inline operation in a method Nordson YesTech calls "human automation." The AOI operator pulls each board from the line as it exits the reflow oven, inspects the board in the benchtop AOI, and then places the board back on the conveyor to continue the process.



Desktop AOI systems offer more flexibility because they can be used to inspect boards throughout different process steps. Courtesy of Nordson YesTech.

According to Biemans, "If you find a problem in an inline system, you can flag it immediately and prevent a larger number of boards from being produced incorrectly before finding the defect. That's the true advantage of inline AOI: You find defects on the spot."

In contrast, with an offline system, you can inspect batch lots while the line is still going, although defects aren't discovered as quickly. Using an offline desktop or AOI system prevents the risk of holding up the entire production line while the inspection program for a new product is still being created or debugged to run the inline AOI system.

One difference between desktop and inline machines that's being erased is in how they are programmed, said Biemans. Many of the big high-volume AOI machines use rule-based programming—inspecting each item on a board, such as a solder joint, requires multiple rules. Image-based programming, more common in desktop machines, uses the actual image to set base targets. To program a specific board on a big inline system could take up to two days, versus two hours for a desktop system. Some of the rule-based systems now have better libraries. In addition, rule-based programming can be added to the Marantz desktop system for certain inspection tasks while keeping the advantages of its original image-based inspection for tasks where that is more efficient and effective.

"In the past five years, we've seen an increase in demand for desktop AOI systems," Biemans said. "They've became more prevalent, cheaper, and much more powerful by combining image-based and rule-based programming architectures. You can now get the same quality in desktop AOI as in inline machines, although their speeds may not have caught up with the fastest inline systems." □

The future of inspection may be mobile

Some machine-vision systems are smaller than traditional benchtops or PCs because they are built on open platforms, not dedicated components, and because embedded and PC architecture, components, and software are becoming more similar. Increasingly powerful components in compact, off-the-shelf systems make it easier to bring machine vision to places where there's less space, said Kamalina Srikant, National Instruments' vision product manager.

"Smart cameras, for example, can now do what it took a desktop PC to do in the past," Srikant said. "Compact machine-vision hardware ranges from smart cameras with integrated image sensors to embedded vision systems with external camera connectivity." For example, NI's Embedded Vision System is a dedicated machine-vision controller with a multicore processor, a real-time OS, FPGAs, and isolated I/O lines. It can be used with multiple IEEE 1394a or GigE Vision tethered cameras.

Compact embedded vision systems can be deployed for wafer sorting or PCB inspection. Courtesy of National Instruments.

Since laptops are becoming more powerful, their hardware no longer limits their use as a vision-system controller, said Nathan Cohen, sales manager for Imperx. He added that the only thing you can't get for laptops are image-processing boards that do real-time high-performance processing in an onboard FPGA, because such boards cannot fit into a laptop. On the other hand, Imperx' laptop frame-grabber card contains drivers for using most software packages. "Now, you can base a machine-vision system on a laptop with two digital camera inputs," said Cohen. One type of portable system in which a laptop and multiple cameras are commonly used is a 3-D data-acquisition system for stereo photogrammetry of large objects.

Because hardware platforms are made in such a compatible way, which one you select for machine vision has become almost transparent, said Endre Toth, director of business development for Vision Components. And you can port an in-house, embedded application based on C or C++ to many different hardware platforms. "So, when you go to design the next generation of inspection or metrology equipment, you can choose a different platform, such as embedded or portable hardware, because it's lower cost, more integrated, and more rugged than earlier hardware generations," he said.

An example of this principle occurred when MVTec ported its Halcon machine-vision software library to the Nokia N900 cellphone and ran a machine-vision application on the phone. Although the relatively poor quality of the optics makes cellphones unsuitable for many industrial machine-vision applications, tasks such as scanning bar codes and data codes, OCR (optical character recognition), and to some extent pattern recognition are feasible, said Heiko Eisele, president of the Germany-based MVTec's US subsidiary.

Traditionally, most machine-vision applications developed with third-party, hardware-independent software have been created for PCs, but in principle these applications can be run on any hardware. "We've made our Halcon machine-vision software available on smart cameras," said Eisele, "and we are getting requests to port it to other embedded platforms, such as compact image-processing systems without all the usual PC peripherals or motherboards, which will be assembled into finished products by our customers."—*Ann R. Thryft*

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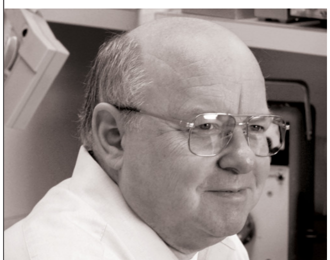
VIEWPOINT

[An exclusive interview with a technical leader]



BRUCE HOFER
Chairman and Co-founder
Audio Precision
Beaverton, OR

Bruce Hofer co-founded Audio Precision in 1984 with a group of audio engineers from the labs of Tektronix. In addition to serving as board chair, Hofer remains technically active as the company's principal analog design engineer. He has received 13 patents, authored many articles and papers, and in 1995 received the Fellowship Award from the International Audio Engineering Society. Hofer earned his BSEE degree from Oregon State University in 1970.

Contributing editor Larry Maloney conducted a phone interview with Bruce Hofer on changes in the audio test field brought on by the expanding variety of consumer electronic products.

How new products challenge audio test

Q: What are the biggest changes in audio test since your company was founded?

A: The biggest change has been the move from analog to digital storage. When we started in 1984, LP records were still the most popular form of serious music. But about the same time, the compact disc and the personal computer were also coming onto the scene. Both caused profound changes in audio test. For example, the PC soon became a powerful force as a test-instrument controller, replacing expensive HP-IB or GPIB-based testers that often required a software engineer for programming. At Audio Precision, we immediately seized on the PC and made it a part of our product offering. By embracing the PC, I believe Audio Precision led the way in automating audio test.

Q: What are Audio Precision's fastest-growing applications?

A: Testing for HDMI (high-definition multimedia interfaces), Dolby, and DTS (digital theater systems). These applications are being driven by multichannel sound, typically five- to seven-channel, surround-sound systems. Consumer devices have embraced HDMI as a virtual standard interface. We've gotten heavily involved not so much in testing the HDMI interface itself, but in analyzing how audio passes through the interface and appears on a device that reproduces the sound or, conversely, in analyzing how a device that is recording the sound or taking it from another source encodes it and puts it onto the HDMI bus.

Q: How are you changing your equipment to meet the needs of customers who do not have strong backgrounds in audio test?

A: It all starts with the user interface, which has changed significantly from our past products. Earlier products were very hardware-centric and designed for audio engineers who really understood audio measurements. So, you got multiple panels for controlling the signal generator, analyzer, sweep engine, and various options. In contrast, our newer products are much more measurement- or result-oriented. When you use our new APx family, the first thing you do is indicate what you want to measure, such as signal-to-noise ratio, and the instrument automatically sets up and performs the test. This easy-to-use interface is especially important, as our testers get used by engineers all around the world.

Q: What has been your most significant product introduction of the past year?

A: It is actually an option, called the BW52, which adds a faster ADC to our APx520 family of analyzers. This option extends the analyzer's capability from 90 kHz to 1 MHz. This allows you to see the full spectrum of the signal. What is driving the need for this option is the growth in class D power amplifiers, which switch at frequencies of 200 to 300 kHz. R&D engineers need to see what that switching frequency is and how much of it is in the signal, as well as how you modulate switches to minimize distortion. One of the applications we're targeting for this new option is automotive, where most of the multichannel power amplifiers are class D. Still another key application is converter testing.

Q: How about major product announcements for 2010?

A: At the recent Audio Engineering Society show in London, we introduced the APx515, a two-channel audio analyzer for production test. We put a big focus on value engineering so we could offer a product that sells for thousands less than our lowest-priced analyzer. Target applications include power amplifiers and home theater products. Although most of our testers are used in product development and quality assurance, we expect the APx515 will trigger more growth in our production test business. T&MW

Bruce Hofer answers more questions about trends in audio test in the online version of this interview: www.tmworld.com/2010_06.

To read past Viewpoint columns, go to www.tmworld.com/viewpoint.